T-BERD® 310

Communications Analyzer User's Guide

TTC™
A Dynatech Company

S.W. BELL- SPL. SVCS. XI515
3311 THOUSAND OAKS
S.A. TX

ML12067
Rev. E

T-BERD 310
COMMUNICATIONS ANALYZER
USER'S GUIDE

SEPTEMBER 1994

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INTRODUCTION

T-BERD 310 Options

INTRODUCTION

The *T-BERD 310 User's Guide* offers an easy, direct method to setup and operate the T-BERD 310 within your network. It presents the most often used test setups in complete and concise steps. Illustrations, helpful notes, and step-by-step procedures make this user's guide a valuable tool for new and experienced users.

This user's guide is designed for the user who needs to know the basics about setting up and operating the T-BERD 310 in a short amount of time. If you are unfamiliar with the instrument, please refer to the *T-BERD 310 Reference Manual* for more detailed information. If you should require additional help, call TTC Customer Service at (800) 638-2049.

The T-BERD 310 help card functional block diagram appears on the last page of the manual for your convenience.

1.1 T-BERD 310 OPTIONS

This user's guide contains applications for the following T-BERD 310 options. The options used are identified at the beginning of the application. One or more of the options may be used in a single application.

- 310-1 DS1/DS0 Analyzer Option
- 310-2 E1 Drop Option
- 310-3 DS1 Insert Option
- 310-4 SONET Drop (STS-1) Option
- 310-4A SONET Drop (STS-1, OC-1/3) Option
- 310-5 DS3 Jitter Option
- 310-6 IEEE-488 Option
- 310-9A Enhanced ESF/DS1 Timing Slips Option
- 310-10 G.821 Results Option
- 310-12 SONET OC-12 Transmit/Receive Option
- 310-13R SONET STS-1 Receive Option
- 310-13T SONET STS-1 Transmit Option
- 310-14R SONET STS-1, OC-1, OC-3 Receive Option
- 310-14T SONET STS-1, OC-1, OC-3 Transmit Option

CONNECTIONS AND TEST SETUPS

T-BERD 310 Connections

Generating Printouts

Timed Test Setups

CONNECTIONS AND TEST SETUPS

2.1 T-BERD 310 CONNECTIONS

Figure 2-1 shows the location of the T-BERD 310 front-panel connections for transmitting and receiving DS3 signals. The PRIMARY DS3 TRANSMIT OUTPUT and PRIMARY DS3 RECEIVE INPUT jacks can be used to connect the T-BERD 310 to a DS3 circuit at several DS3 access points which can include the DS3 multiplexer, the DSX-3 patch panel, and the DS3 side of a long-haul transmission system. Figure 2-2 identifies the typical access points where you can connect the T-BERD 310 for circuit and network testing. Table 2-1 lists the T-BERD 310 transmit and receive connection and level settings for the access points identified in Figure 2-2.

Along with the front-panel connections, your T-BERD 310 may have one or more of the side-panel connections shown in Figure 2-3. The side-panel connections enable the T-BERD 310 to transmit DS3 and DS1 signals; drop out DS1, E1, DS0, and VF signals to external test sets; analyze DS3 signals, DS1 signals, and SONET overhead from STS-1, OC-1, OC-3, OC-3c, and OC-12 signals; analyze both sides of a DS3 line; insert and test a DS1 channel in a live DS3 signal out; and analyze the amplitude and frequency components of jitter. STS-, OC-1, OC-, OC-3, OC-3c, and OC-12 signal puts are also available to test SONET circuits.

The following side-panel connections come standard on the T-BERD 310 mainframe.

RS-232 interface connector — 25-pin D connector for printer or remote control operation.

MULTIPLE DS3 OUTPUT jacks — WECO 560 jacks (5 each) with the same output as the PRIMARY DS3 TRANSMIT OUTPUT jack.

DS1 DROP jack — WECO 310 jack which enables a DS1 signal to be dropped from either the primary DS3 receive input signal or a SONET drop option.

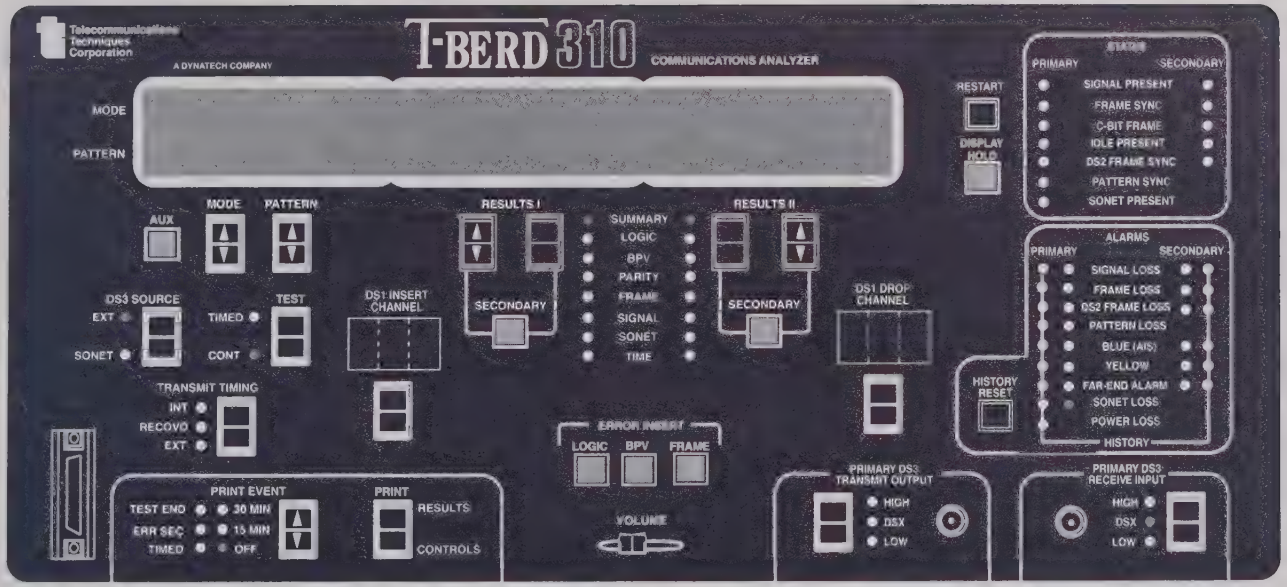


Figure 2-1
T-BERD 310 Front Panel

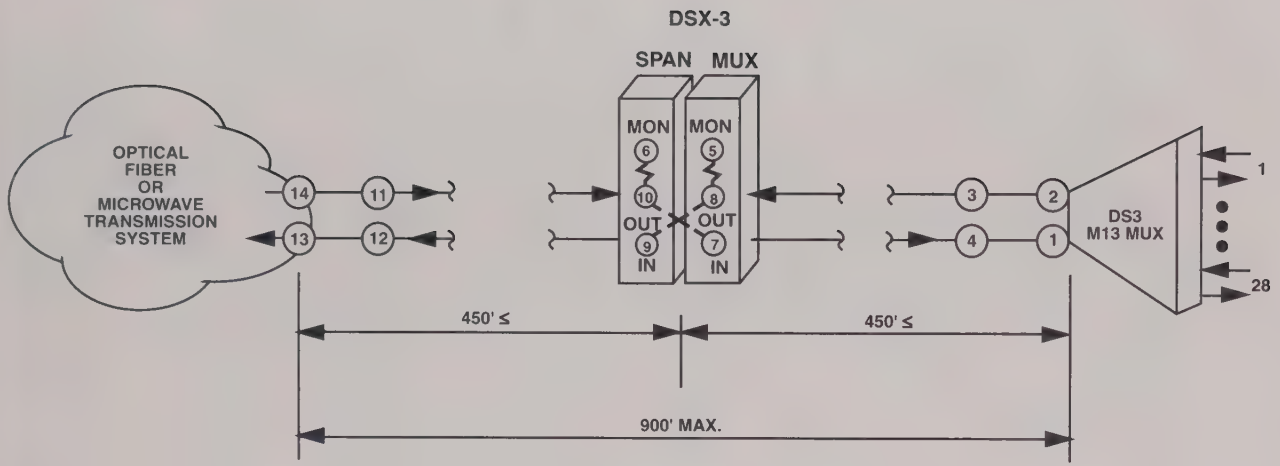

DSX-3
SPAN MUX
MON
MON
6
5
10
8
OUT
OUT
9
7
IN
IN
OPTICAL
FIBER
OR
MICROWAVE
TRANSMISSION
SYSTEM
14
11
13
12
3
2
4
1
DS3
M13 MUX
1
28
450' ≤
450' ≤
900' MAX.

Table 2-1
T-BERD 310 DS3 Connections and Level Settings

Connections		Switch Settings		Description
TX	RX	TX	RX	
1	2	LOW[1]	HIGH	Connected across IN/OUT of multiplexer.
3	4	HIGH	LOW[1]	Connected across IN/OUT of cable, in place of the multiplexer.
—	5	—	DSX	Connected at MUX DSX-3 MON jack.
—	6	—	DSX	Connected at SPAN DSX-3 MON jack.
7	8	DSX	DSX	Connected across MUX DSX-3 IN/OUT jacks.
9	10	DSX	DSX	Connected across SPAN DSX-3 IN/OUT jacks.
11	12	HIGH	LOW[1]	Connected across IN/OUT of cable, in place of the transmission system.
13	14	LOW[1]	HIGH	Connected across IN/OUT of transmission system.

[1] Use DSX if the cable length is less than 200 feet from the DSX-3 patch panel.

EXT CLOCK connector — BNC connector which enables an external input for a DS3 level clock source.

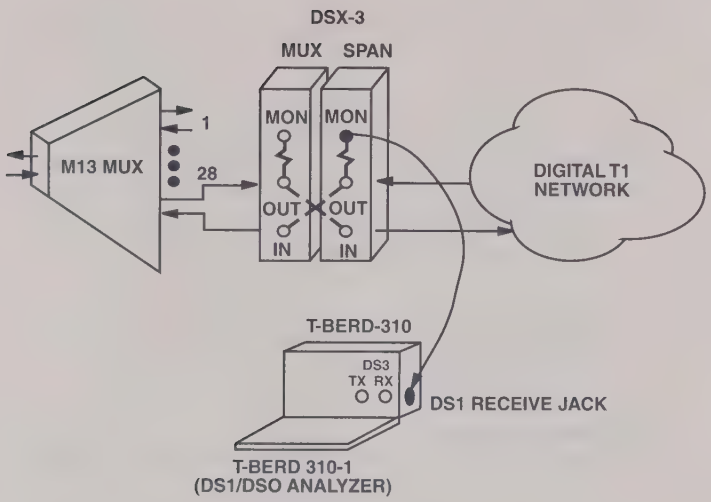


Figure 2-3
T-BERD 310 Side-Panel Connections

The following side-panel connections are available on the indicated option.

310-1 DS1/DS0 Analyzer Option

VF OUT jack — WECO 310 jack with a 600 ohm terminated analog output.

DS1 TRANSMIT jack — WECO 310 jack with a DS1 output.

DS1 RECEIVE jack — WECO 310 jack for a DS1 input.

DATAPORT connector — 9-pin D connector which enables a DS0 channel or datalink (ESF, ESFz, or SLC) output.

310-2 E1 Drop Option

E1 DROP jack — 3-prong banana jack which enables an E1 signal to be dropped from either the primary DS3 receive input signal or a SONET DS3 payload.

310-3 DS1 Insert Option

DS1 INSERT INPUT jack — WECO 310 jack to insert a DS1 signal into a secondary DS3 signal.

SECONDARY DS3 RECEIVE jack — WECO 560 jack for a second DS3 input.

310-4 SONET Drop (STS-1) Option

STS-1 RECEIVE jack — WECO 560 jack for a STS-1 level electrical input.

310-4A SONET Drop (STS-1, OC-1/3) Option

STS-1 RECEIVE jack — WECO 560 jack for a STS-1 level electrical input.

OC-1/3 RECEIVE connector — FC(PC) connector for an OC-1 or OC-3 level optical input.

310-5 DS3 Jitter Option

JITTER OUTPUT jack — WECO 560 jack with a demodulated output signal.

310-6 IEEE-488 Option

IEEE-488 interface connector — IEEE-488 connector for printer or remote control operation

310-12 SONET OC-12 Transmit/Receive Option

OC-12 TRANSMIT connector — Selectable optical connector for an OC-12 optical output.

OC-12 RECEIVE connector — Selectable optical connector for an OC-12 optical intput.

310-13R SONET STS-1 Receive Option

STS-1 RECEIVE connector — WECO 560A connector for an STS-1 electrical input.

DCC DROP INSERT connector — RS-449 compatible, 15-pin, D-type female connector for Line and Section DCC access.

310-13T SONET STS-1 Transmit Option

STS-1 TRANSMIT connector — WECO 560A connector for an STS-1 electrical output.

DS1 BITS CLOCK jack — Bantam jack for DS1 BITS clock input.

HANDSET jack — RJ-11 jack for orderwire channel handset.

310-14R SONET STS-1, OC-1, OC-3 Receive Option

STS-1 RECEIVE connector — WECO 560A connector for an STS-1 electrical input.

OC-1/OC-3 RECEIVE connector — Selectable optical connector for an OC-1 or OC-3 optical input.

DCC DROP INSERT connector — RS-449 compatible, 15-pin, D-type female connector for Line and Section DCC access.

310-14T SONET STS-1, OC-1, OC-3 Transmit Option

STS-1 TRANSMIT connector — WECO 560A connector for an STS-1 electrical output.

OC-1/OC-3 TRANSMIT connector — Selectable optical connector for an OC-1 or OC-3 optical output.

DS1 BITS CLOCK jack — Bantam jack for DS1 BITS clock input.

HANDSET jack — RJ-11 jack for orderwire channel handset.

2.2 GENERATING PRINTOUTS

Use the following information to configure the T-BERD 310 and compatible printer, such as the TTC PR-40A Thermal Printer, to generate *results* and *controls* printouts. You can connect either an RS-232 or IEEE-488 compatible printer to the T-BERD 310. The printer connections are found on the side panel.

Perform the following procedure to set up the T-BERD 310 to generate *results* and *controls* printouts. If a printer is not available, you can still generate printouts by storing them in the internal print buffer. This procedure assumes you know how to setup the printer for proper operation (refer to the printer operating manual for operating procedures).

AUX/MODE/PATTERN switches

Set the PRINT auxiliary group functions as follows:

Auxiliary Function	Selections	Comments
Printout Control		
INTERVAL	00:01 to 24:59	Set the **PRINT EVENT** switch to TIMED.
MODE	CONTINUOUS DELTA	Determines whether test results are or accumulated throughout the test or are only accumulated between print events.
FORMAT	NORMAL, CUSTOM, or SUMMARY	Determines what results format is printed.
CUSTOM		Selects the results to be included in the custom *results* printout. Select the SUMMARY category to set the desired Status and Alarm LEDs and Far-End Alarm messages. Select the other categories to select the desired results.
WIDTH	40 or 80	Sets the printout line width.
RS-232 and IEEE-488 Interface Control		
BAUD RATE	110, 300, 600, 1200, 2400, 4800, or 9600	Sets the RS-232 interface baud rate.
PARITY	NONE, ODD	Sets the RS-232 interface parity. Set or EVEN parity to NONE when printing pulse shape graphs.
TERMINATOR	CR, LF, or CRLF	Sets printout line terminator. Set the terminator to CR when printing pulse shape graphs.
PORT	RS-232, IEEE-488, or IEEE-488 Talk-only	Selects printer interface port. This Addressable function only appears when the 310-6 IEEE-488 Option is installed.

2. **AUX switch**

Exit the auxiliary functions.

1. **Connect a printer to the T-BERD 310 (RS-232 or IEEE-488)**

4. **PRINT switch**
   Generate either a *results* or *controls* printout to verify the proper operation of the printer and T-BERD 310.

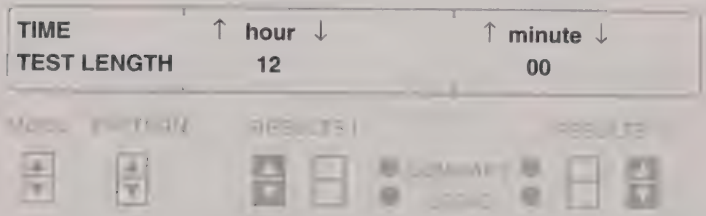
5. **PRINT EVENT switch**
   Select the necessary print event function to generate the appropriate *results* printout.

2.3 TIMED TEST SET UP

This procedure enables you to run an unattended test for an extended period and collect test results during and after the test. Perform the following procedure to set up the T-BERD 310 for a timed test and print the *results* at the end of the test. Specific results printouts are generated during the test by selecting the desired print event function with the **PRINT EVENT** switch.

1. **Connect compatible printer (optional)**
   Refer to Section 2.2 to connect a printer.

2. **AUX/MODE/PATTERN switches**
   Select the TEST LENGTH auxiliary function to set the test length.



4. **AUX switch**
   Exit the auxiliary functions.

PRINT EVENT switch (optional)

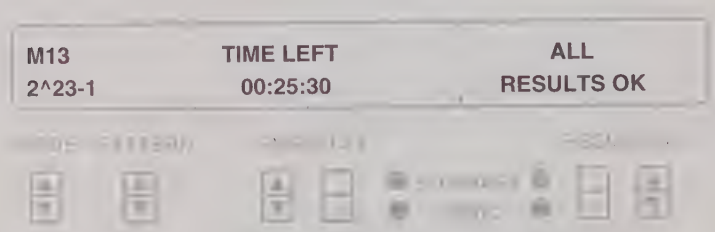
Select the TEST END to generate the test end *results* printout at the end of the test. The test end *results* printout can also be printed from the other print event functions simply by setting the **TEST** switch to TIMED.

TEST switch

Select the TIMED test (changing from CONT to TIMED restarts the test).

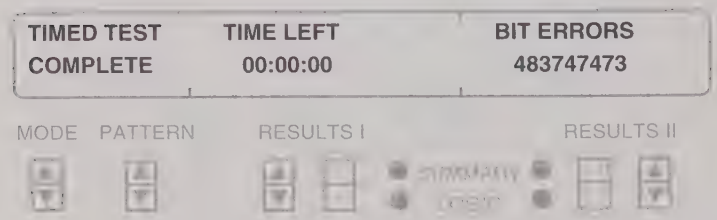
Display timed test results

Select the TIME category TIME LEFT result in the RESULTS I window and the SUMMARY category in the RESULTS II window.



T-BERD 310 displays completed timed test results

When the result equals 00:00:00, the test is complete, "TIMED TEST COMPLETE" flashes in the display, and the test result counts are frozen.



8. **Evaluate the test results**

When the test is complete, evaluate the results by either scrolling through the frozen results or scanning the printouts.

IN-SERVICE SIGNAL MONITORING

DS3 Monitoring

Bidirectional DS3 Monitoring

DS1, E1, and DS0 Monitoring from DS3 Access Points

DS1/DS0 Monitoring from DS1 Access Points

IN-SERVICE SIGNAL MONITORING

3.1 DS3 MONITORING

- Determine the performance of a live DS3 circuit in one direction without disrupting service.
- Monitor the DS3 signal for BPVs, frame errors, C-bit errors, parity errors, and Far-End Alarm messages.
- Measure the DS3 signal frequency.

Figure 3-1 illustrates how the T-BERD 310 connects to the DS3 circuit to analyze live data.

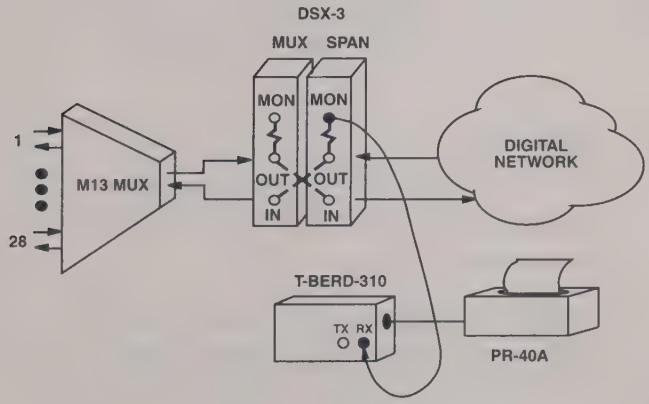


Figure 3-1
Monitoring DS3 Network Performance

Connect a compatible printer (optional)

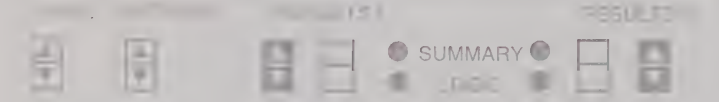
DS3 SOURCE switch
Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

MODE switch
Select AUTO.

TEST switch
Select CONT or TIMED.

AUX/MODE/PATTERN switches
Select the BEEP CRI auxiliary function to select the beep criteria.

MISC	↑ select ↓	↑on off↓
BEEP CRI	PATT SYNC	OFF



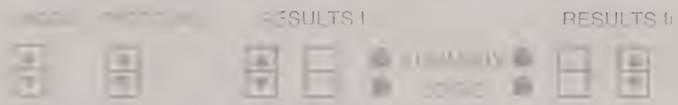
AUX switch
Exit the auxiliary functions.

VOLUME switch
Set to middle position.

PRIMARY DS3 RECEIVE INPUT switch and jack
Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

MODE/PATTERN window
Verify the framing format and pattern.

c-bit	ALL	BPV %EFS
live	RESULTS OK	100.00%



RESTART switch
Clear the old test results and start a new test.

Primary Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync (if applicable).

RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

Results Interpretation

When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

BPV Category

BPV results — BPVs indicate problems with the local office equipment where the signal is being monitored. Since a BPV always causes a bit error, monitoring for BPVs provides an estimate of the number of bit errors occurring on an in-service line.

BPV THR ES — BPV threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERROR THR auxiliary function. This

allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

PARITY Category

P-bit parity results (M13 and C-bit parity framing formats) — P-bit parity indicates the parity of the previously transmitted DS3 frame, and it is recalculated at each intermediate step in the transmission path by higher-order transmission systems. Therefore, P-bit parity results indicate signal integrity only on the last monitored leg of the transmission span.

C-bit parity results (C-bit parity framing format only) — C-bit parity is calculated only by terminating DS3 equipment at each end of the network, allowing C-bit parity results to indicate signal integrity from end to end.

Far-End Block Errors (FEBEs) results (C-bit parity framing format only) — If a C-bit parity or frame error is detected by the far-end equipment, the equipment detecting the error sends a FEBE back to the near end.

> Monitoring C-bit parity errors *and* FEBEs simultaneously allows both directions of the span to be evaluated from one location with one test set. If C-bit parity errors are being received, errors are being caused by the return leg of the DS3 span. If FEBEs are being received, errors are being caused on the transmitting leg of the DS3 span.

FRAME Category

Frame error results — Since the DS3 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS3 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

FEOOF SEC — Far-End Out-Of-Frame Seconds indicate that the DS3 equipment in the far-end direction has lost frame synchronization with the signal being transmitted from the near-end direction. This condition is also known as a Yellow Alarm or Remote Alarm Indication (RAI). A Yellow Alarm is transmitted by setting the X-bits to 00, and is applicable only with the C-bit parity framing format.

NEOOF SEC — Near-End Out-Of-Frame Seconds indicate that the T-BERD 310 has lost frame synchronization with the received DS3 signal or has received a Blue Alarm (AIS). A near-end out-of-frame condition exists when excessive bit errors are occurring on the DS3 line, therefore corrupting the framing sequence.

DS2 FRM ERR — If the DS3 signal is channelized (the signal contains DS1, DS2, and DS3 framing bits), the DS2 and DS3 framing bits can be monitored for bit errors occurring in the DS3 payload. Monitoring DS2 frame errors also aids in isolating the cause of the errors between the DS3 and DS1 levels.

FRM THR ES — Frame threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

SIGNAL Category

RX FREQ — An out-of-range frequency could indicate that a timing source is bad, or that the timing source cannot recover the clock rate from the DS3 signal. The clock rate may not be recoverable if the DS3 signal does not maintain the 33% ones density rule, which could be caused by equipment improperly implementing B3ZS encoding. Also, since higher-order transmission equipment should not alter the DS3 frequency, an out-of-range frequency could be caused by DS3 transmission equipment such as a DS3 multiplexer.

Pulse shape results — The pulse shape can be monitored for changing trends in the signal performance. Refer to Section 6.1 to measure the pulse shape.

DS3 jitter results — Wideband and highband jitter can be monitored to isolate sources of DS3 jitter. Refer to Section 7 to measure the wideband and highband jitter.

3.2 BIDIRECTIONAL DS3 MONITORING

- Determine the performance of a live DS3 circuit in both directions without disrupting service.
- Monitor the DS3 signal for BPVs, frame errors, C-bit errors, parity errors, Far-End Block Errors, and Far-End Alarm messages on the primary and secondary sides of the DS3 circuit.
- Measure the DS3 signal frequency on the primary and secondary sides of the DS3 circuit.
- Requires the 310-3 DS1 Insert Option

Figure 3-2 illustrates how the T-BERD 310 connects to the DS3 circuit to analyze live data on both sides of the line.

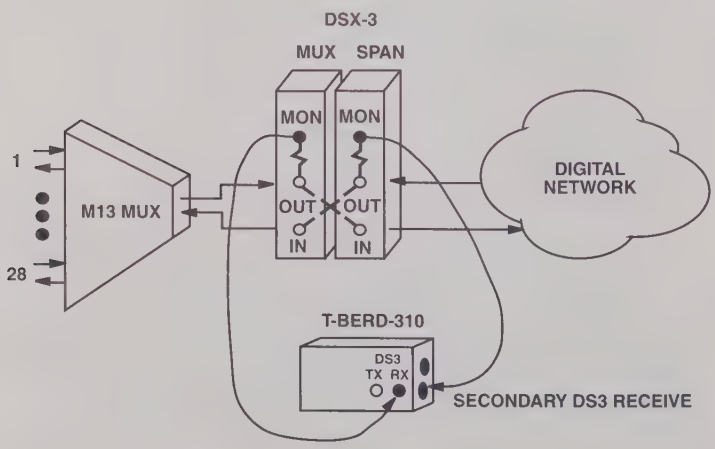


Figure 3-2
Monitoring Both Sides of a DS3 Line

Connecting and monitoring the primary DS3 signal

Perform the procedure in Section 3.1 to configure the T-BERD 310 mainframe for the primary side of the line.

SECONDARY DS3 RECEIVE jack (side panel)

Plug a cable between this jack and the span-side MONitor jack.

RESTART switch

Clear the old test results and start a new test.

Secondary Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync (if applicable).

RESULTS II test results (secondary)

Select the secondary SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

> The T-BERD 310 is equipped with an audible alarm that beeps when the error criteria are met. The audible alarms provide immediate notification that the intermittent error has occurred. Set the beep criteria with the BEEP CRI auxiliary function.

Results Interpretation

Using dual DS3 receivers to monitor both sides simultaneously insures that the next error to occur is observed, minimizing test time. After looking at the error results for the primary and secondary DS3 receivers, the source direction that received the error can then be monitored using the primary DS3 receiver for complete in-service troubleshooting. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

Secondary Results

The C-BIT ERRORS, PAR ERRORS, FEBE, FRM ERRORS, VIOLATIONS, RX FREQ, and FEAC Code results that are used for performing in-service DS3 monitoring are also applicable to in-service bidirectional DS3 monitoring. However, the prime use for dual DS3 receivers is to isolate the source direction of intermittent errors.

Primary Results

Once the source direction is known, the T-BERD 310 primary DS3 receiver can be used to troubleshoot the problem in the appropriate direction as described in Section 3.1.

3.3 DS1, E1, AND DS0 MONITORING FROM DS3 ACCESS POINTS

- Determine the performance of a live DS1 or E1 circuit from a DS3 access point without disrupting service.
- Monitor the DS1 signal for frame errors and CRC errors.
- Measure the DS1 signal frequency.
- Monitor DS0 channel signaling and VF level.
- Drop an E1 channel to an E1 test set to analyze the E1 signal.
- Requires either the 310-1 DS1/DS0 Analyzer Option, an external DS1/DS0 test set (e.g., the TTC T-BERD 211), or 310-2 E1 Drop Option and external E1 test set (e.g., the TTC INTERCEPTOR 1402).

Figure 3-3 illustrates how the T-BERD 310 connects to the DS3 circuit to monitor and analyze the DS1/DS0 live data and drop an E1 channel.

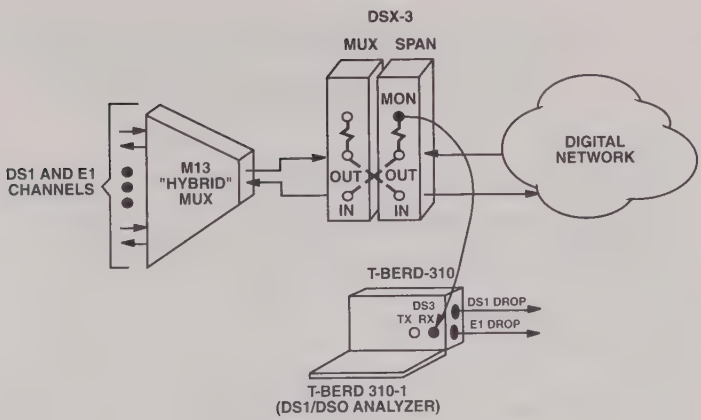


Figure 3-2
Monitoring DS1/DS0/E1 Channels from the DSX-3 Patch Panel

T-BERD 310 Mainframe Setup

Connecting and monitoring the DS3 signal

Perform the procedure in Section 3.1 to configure the T-BERD 310 mainframe.

T-BERD 310 DS1 DROP CHANNEL switch

Select the desired DS1/E1 channel to be monitored.

- To analyzes the DS1 and DS0 channels, continue with the *310-1 DS1/DS0 Analyzer Option Setup* procedure. The DS1 channels appear as 1 to 28 in the DS1 DROP CHANNEL window.

- To analyze the DS1 channels with an external DS1 test set, continue with the *External DS1 Test Set Setup* procedure. The DS1 channels appear as 1 to 28 in the DS1 DROP CHANNEL window.

To analyze the E1 channels, continue with the *310-2 E1 Drop Option Setup* procedure. The E1 channels appear as E1 to E21 in the DS1 DROP CHANNEL window.

310-1 DS1/DS0 Analyzer Option Setup

310-1 DS1 SOURCE switch
Select DS3 DROP (DS1 dropped from the T-BERD 310).

310-1 MODE switch
Select AUTO.

RESTART switch
Clear the old test results and start a new test.

310-1 Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, and B8ZS (if applicable).

310-1 MODE/PATTERN window
Verify the framing format and pattern.

t1 d4	ALL	FRM ERRORS
live	RESULTS OK	0

310-1 RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

External DS1 Test Set Setup

T-BERD 310 DS1 DROP jack (side panel)
Connect the DS1 test set to this WECO 310 jack.

T-BERD 310 AUX/MODE/PATTERN switches (optional)
If a SONET drop option is installed, set the DS1 DROP OUT auxiliary function to DS3. This drops the DS1 channel to the DS1 DROP jack from the DS3 signal.

SONET	**↑ select ↓**
DS1 DROP OUT	**DS3**

310-1 AUX switch
Exit the auxiliary functions.

DS1 test results
Refer to the DS1 test set operating manual for signal analysis capabilities.

310-2 E1 Drop Option Setup

T-BERD 310 E1 DROP jack (side panel)
Connect the E1 test set to this 3-prong banana jack.

E1 test results
Refer to the E1 test set operating manual for signal analysis capabilities.

310-1 Results Interpretation

When monitoring a DS1 signal and DS0 channels from a DS3 access point, observe the results in the FRAME and SIGNAL categories.

The BPV category and RX LVL dBdsx result are not applicable since the DS1 channel is dropped internally from within a DS3 signal.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

SIGNAL Category

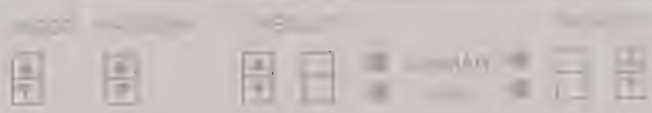
The SIGNAL category results include both DS1 and DS0 measurements.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (1,543,923 to 1,544,077 Hz), the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.

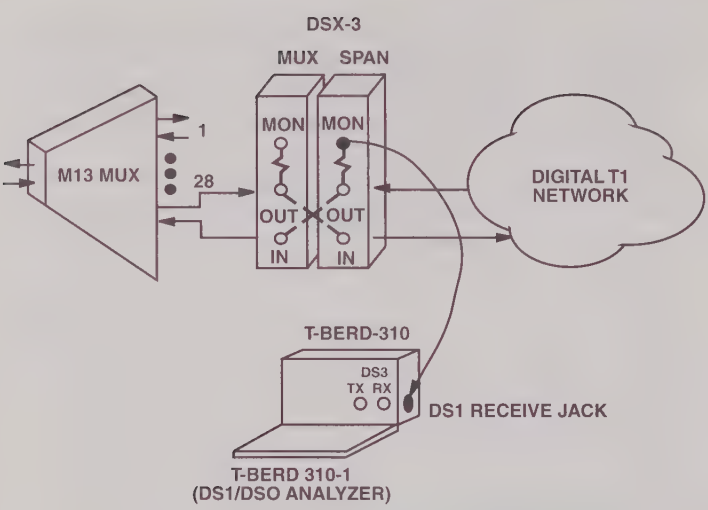
t1 d4	[a] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 [b] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
live	[c] [d] **N/A**



3.4 DS1/DS0 MONITORING FROM DS1 ACCESS POINTS

- Test DS1 channels without having to use another test set.
- Determine the performance of a live DS1 circuit from a DS1 access point without disrupting service.
- Monitor the DS1 signal for BPVs, frame errors, and CRC errors.
- Measure the DS1 signal frequency and DS1 level.
- Monitor DS0 channel signaling and VF level.
- Requires the 310-1 DS1/DS0 Analyzer Option.

Figure 3-4 illustrates how the T-BERD 310 connects to the DS1 circuit to monitor and analyze the DS1/DS0 live data.



1. **310-1 DS1 SOURCE switch**
   Select EXT. INPUT (side-panel DS1 RECEIVE jack).

2. **310-1 MODE switch**
   Select AUTO.

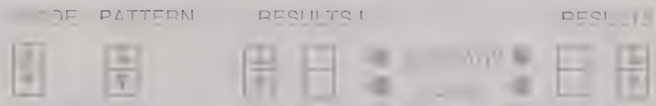
3. **310-1 RECEIVE INPUT switch and DS1 RECEIVE jack (side panel)**
   Select the DSX-MON input level and plug a cable between this jack and the span-side MONitor jack.

4. **310-1 RESTART switch**
   Clear the old results and start a new test.

5. **310-1 Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, and B8ZS (if applicable).

5. **310-1 MODE/PATTERN window**
   Verify the framing format and pattern.

t1 d4	ALL	BPV %EFS
live	RESULTS OK	100.00%



7. **310-1 RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

8. **310-1 DS0 DROP CHANNEL switch**
   Select the desired DS0 channel.

9. **T-BERD 310 VOLUME switch**
   Adjust to hear the DS0 channel.

310-1 Results Interpretation

When monitoring a DS1 signal and DS0 channels from a DS1 access point, observe the results in the BPV, FRAME, and SIGNAL categories.

BPV Category

BPV results — BPVs can be detected since the DS1 signal being analyzed is accessed directly from the DS1 access point. Since a BPV always causes a bit error, monitoring BPVs gives an estimate of the number of bit errors occurring on an in-service line.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

SIGNAL Category

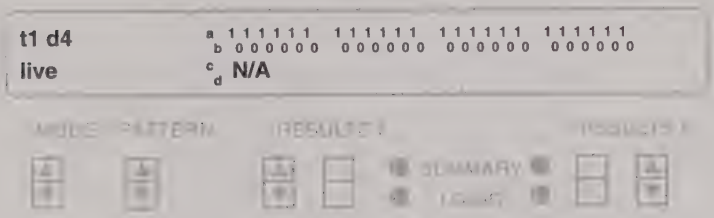
The SIGNAL category results include both DS1 and DS0 measurements.

RX LVL dBdsx — The DS1 receive level can be measured.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (1,543,923 to 1,544,077 Hz), the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.



BERT TESTING

DS3 Loopback BERT Testing at DS3 Access Points

DS1 Loopback BERT Testing at DS1 Access Points

BERT TESTING

4.1 DS3 LOOPBACK BERT TESTING AT DS3 ACCESS POINTS

- Test the performance of a DS3 circuit from a DS3 access point during installation and acceptance testing.
- Loopback the DS3 signal at a far-end to verify circuit continuity.
- Test the DS3 circuit for logic errors, BPVs, frame errors, parity errors, and Far-End Alarm messages.
- Measure the DS3 signal frequency, level, and power.

Figure 4-1 illustrates the test setup with the T-BERD 310 at the near end and the loopback at the far end of the DS3 circuit.

1. **Loopback the far end**
   Loopback the far end of the DS3 span at the DSX-3 patch panel.

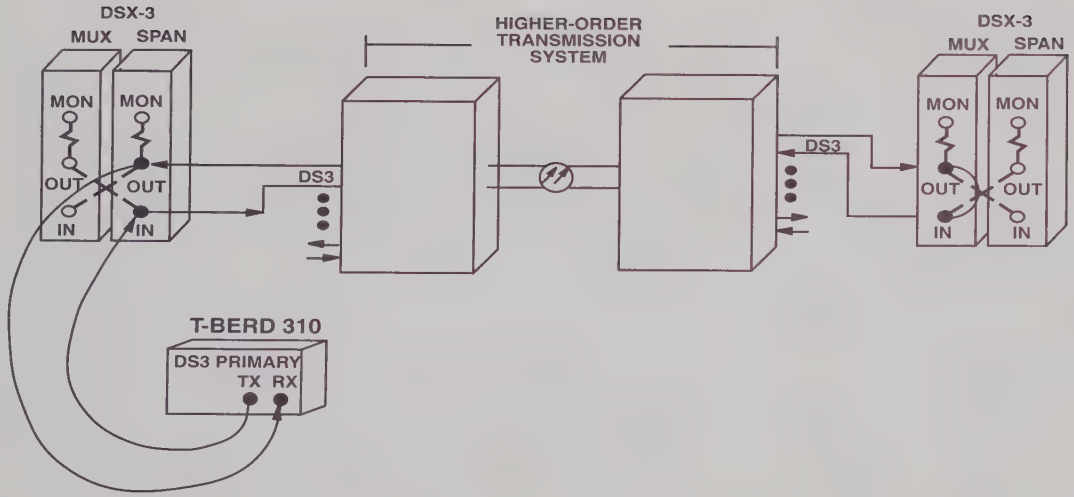
2. **DS3 SOURCE switch**
   Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

3. **MODE switch**
   Select the appropriate framing format, e.g., M13 or C-BIT mode.

4. **PATTERN switch**
   Select the appropriate test pattern, e.g., 2^23-1.

5. **TRANSMIT TIMING switch**
   Select INT.

6. **PRIMARY DS3 RECEIVE INPUT switch and jack**
   Select the DSX input level and plug a cable between this jack and the span-side OUT jack.


DSX-3
MUX
SPAN
MON
MON
OUT
OUT
IN
IN
DS3
HIGHER-ORDER
TRANSMISSION
SYSTEM
DS3
DSX-3
MUX
SPAN
MON
MON
OUT
OUT
IN
IN
T-BERD 310
DS3 PRIMARY
TX
RX

PRIMARY DS3 TRANSMIT OUTPUT switch and jack
Select the DSX output level and plug a cable between this jack and the span-side IN jack.

RESTART switch
Clear the old results and start a new test.

Primary Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and Pattern Sync.

RESULTS I Category switch
Select the SUMMARY category.

LOGIC ERROR INSERT switch
Press this switch quickly several times to send logic errors down the circuit. Verify that the T-BERD 310 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

RESTART switch
Clear the old results and start a new test.

RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

Results Interpretation

When performing an out-of-service DS3 bit error rate test, observe the results in the LOGIC, BPV, PARITY, FRAME, and SIGNAL categories.

LOGIC Category

Bit error results — DS3 bit error rate testing (BERT) involves transmitting a DS3 test pattern into the network, looping the signal back through the network, and comparing the transmitted and received signals bit by bit. Any change in the bit pattern is counted as a bit error. Verification that the test pattern is received back through the network also insures continuity along the entire transmission path. Since logic errors propagate through all transmission equipment, BERT testing can be used to test the end-to-end performance of a transmission system.

BIT THR ES — Bit threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

BPV, PARITY, and FRAME Categories

If bit errors are occurring, the results used for in-service DS3 monitoring can also be used to isolate the error source. Refer to Section 3.1 for additional information.

SIGNAL Category

RX FREQ — An out-of-range frequency could indicate that a timing source is bad, or that the timing source cannot recover the clock rate from the DS3 signal. The clock rate may not be recoverable if the DS3 signal does not maintain the 33% ones density rule, which could be caused by equipment improperly implementing B3ZS encoding. Also, since higher-order transmission equipment should not alter the DS3 frequency, an out-of-range frequency is probably caused by DS3 transmission equipment such as a DS3 multiplexer.

POWER — DS3 power measurements can be used to insure that the network can supply and handle the maximum power requirements. Power measurements should be made using an unframed All Ones DS3 test pattern to insure maximum power usage. A framed All Ones pattern can be used, but the power reading will be up to 5% lower than the maximum power that could occur.

LEVEL — The signal level result indicates whether the transmission equipment is set to the proper line build-out (LBO). Improper LBO settings can cause the DS3 signal to be received either too weak or too strong for the next piece of equipment to handle.

Pulse shape results — The pulse shape can be measured and compared to standard pulse mask specifications. Refer to Section 6.2 to measure the pulse shape during a BERT test.

DS3 jitter results — Wideband and highband jitter can be monitored to isolate sources of DS3 jitter. Refer to Section 7 to measure the wideband and highband jitter.

Error Insertion

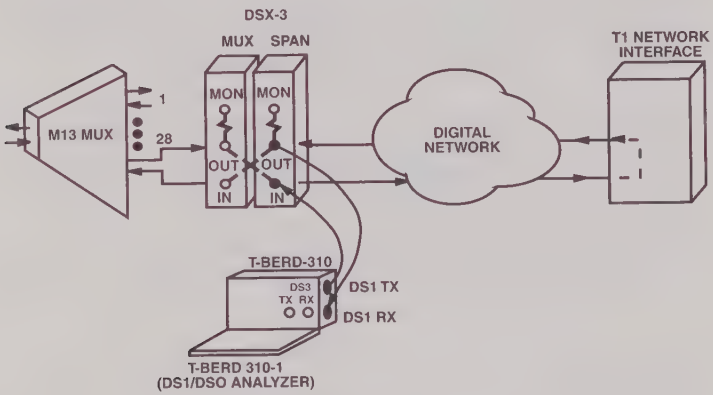
Logic, BPV, and frame error insertion can be used to test DS3 equipment recovery time, equipment tolerance, and alarm and protection switching. Use the **ERROR INSERT** switches and the ERR INSERT auxiliary group to insert controlled errors.

4.2 DS1 LOOPBACK BERT TESTING AT DS1 ACCESS POINTS

- Test the performance of a DS1 circuit from a DS1 access point during installation and acceptance testing.
- Loopback the DS1 signal at a far-end Network Interface Unit (NIU) to verify circuit continuity.
- Test the DS1 circuit for logic errors, BPVs, frame errors, and CRC errors.

- Measure the DS1 signal frequency and level.
- Requires the 310-1 DS1/DS0 Analyzer Option and the 310-9A Enhanced ESF/DS1 Timing Slips Option.

Figure 4-2 illustrates the test setup with the 310-1 DS1/DS0 Analyzer Option connected to the T1 circuit and the NIU is looped back.



310-1 AUX/PATTERN switch

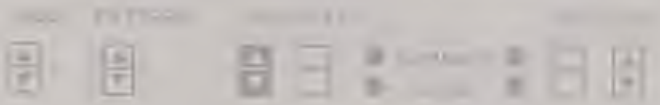
Select the LP CODE auxiliary function to set the appropriate loop code. The in-band loop codes can be used in all framed modes. The ESF out-of-band loop codes can be used in the ESF and ESFz modes.

AUX	↑ in band ↓	↑ out of band ↓
LP CODE	FAC1	LINE

PATTERN switch (optional)

Select the ESF LOOP auxiliary function to set the ESF loop code type.

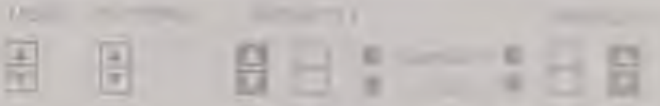
AUX	↑ select ↓
ESF LOOP	IN BAND



PATTERN switch (optional)

Select the PRM auxiliary function to set the ESF or ESFz PRM transmit and receive functions.

AUX	↑prm transmit↓	↑ prm rcvr ↓
PRM	OFF	ON



310-1 AUX switch

Exit the auxiliary functions.

310-1 DS1 SOURCE switch

Select EXT. INPUT (side-panel DS1 RECEIVE jack).

310-1 MODE switch

Select an appropriate framing format, e.g., T1 ESF mode.

310-1 PATTERN switch

Select an appropriate test pattern, e.g., QRSS.

310-1 TRANSMIT TIMING switch
Select INTERNAL.

310-1 CODE switch
Select AMI or B8ZS encoding.

310-1 RECEIVE INPUT switch and DS1 RECEIVE jack (side panel)
Select the TERM input level and plug a cable between this jack and the span-side OUT jack.

310-1 DS1 TRANSMIT jack (side panel)
Plug a cable between this jack and the span-side IN jack.

310-1 LOOP UP switch
Transmit the selected loop-up code. When the loopback is accomplished, the switch LED goes off and the loop code message is replaced with the selected test pattern.

310-1 RESULTS I Category switch
Select the SUMMARY category.

310-1 LOGIC ERROR INSERT switch
Press this switch quickly several times to send logic errors down the circuit. Verify that the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

310-1 RESTART switch
Clear the old results and start a new test.

310-1 Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, Pattern Sync, and B8ZS (if applicable).

310-1 RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 Results Interpretation

When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories.

LOGIC Category

Bit error results — DS1 bit error rate testing (BERT) involves transmitting a DS1 test pattern into the network, looping the signal back through the network, and comparing the transmitted and received signals bit by bit. Any change in the bit pattern is counted as a bit error. Verification that the test pattern is received back through the network also insures continuity along the entire transmission path. Since logic errors propagate through all transmission equipment, BERT testing can be used to test the end-to-end performance of a transmission system.

BIT THR ES — Bit threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

BPV, FRAME, and SIGNAL Categories

If bit errors are occurring, the results used for in-service DS1 monitoring can also be used to isolate the error source. Refer to Section 3.4 for additional information.

INSERTING DS1 SIGNALS INTO LIVE DS3 SIGNALS

DS1 Insert Option Signal Flow

Inserting an Internal DS1 Signal into a Live DS3 Signal

Inserting an External DS1 Signal into a Live DS3 Signal

INSERTING DS1 SIGNALS INTO LIVE DS3 SIGNALS

5.1 DS1 INSERT OPTION SIGNAL FLOW

The 310-3 DS1 Insert Option allows the T-BERD 310 to insert a DS1 channel into a live multiplexed DS3 signal. The option equips the T-BERD 310 with a secondary DS3 receiver and a DS1 receiver.

Figure 5-1 illustrates the signal flow when performing DS1 drop and insert testing. A DS1 signal is inserted into a selected channel of the secondary DS3 receive input. The DS1 signal can be sourced internally from the 310-1 DS1/DS0 Analyzer Option, or externally from the DS1 insert input. Once the DS1 channel is inserted into the DS3 signal, the full DS3 is transmitted into the network. The DS1 channel can then be looped back into the returning DS3 signal. This DS3 signal is then accepted by the primary DS3 receive input. The DS1 channel can then be dropped and analyzed by either the 310-1 DS1/DS0 Analyzer Option or by an external DS1 test set.

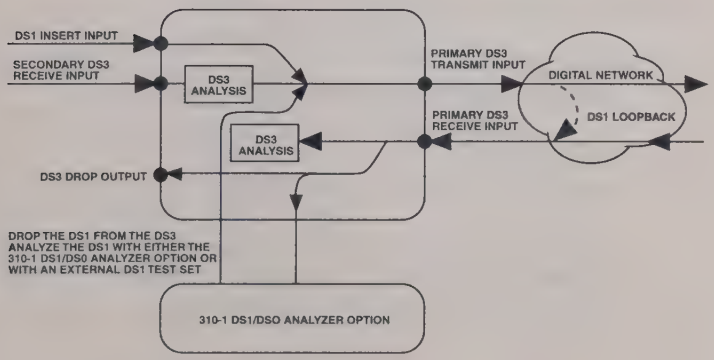

DS1 INSERT INPUT
SECONDARY DS3 RECEIVE INPUT
DS3 ANALYSIS
PRIMARY DS3 TRANSMIT INPUT
DIGITAL NETWORK
PRIMARY DS3 RECEIVE INPUT
DS1 LOOPBACK
DS3 ANALYSIS
DS3 DROP OUTPUT
DROP THE DS1 FROM THE DS3 ANALYZE THE DS1 WITH EITHER THE 310-1 DS1/DS0 ANALYZER OPTION OR WITH AN EXTERNAL DS1 TEST SET
310-1 DS1/DSO ANALYZER OPTION

Figure 5-1
DS1 Insert Option Signal Flow Diagram

5.2 INSERTING AN INTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

- Access a live DS3 signal and drop and insert a DS1 signal from an internal source.
- Perform an out-of-service loopback test on a DS1 channel of a live DS3 signal.
- Insert an internally generated DS1 test pattern or loop code.
- Perform a bit error rate test on the out-of-service DS1 channel.
- Requires the 310-3 DS1 Insert Option and the 310-1 DS1/DS0 Analyzer Option.
- Requires a 75 ohm terminator.

NOTE When this procedure is performed properly, the DS3 signal is unaffected and only one DS1 channel is placed out of service.

Figure 5-2 shows the T-BERD 310 connected to the DSX-3 patch panel. The 310-1 DS1/DS0 Analyzer Option provides the inserted DS1 channel test pattern and DS1 analysis capabilities.

T-BERD 310 Mainframe Setup

1. **DS3 SOURCE switch**
   Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

2. **MODE switch**
   Select the DS1 INSERT mode. Transmit timing defaults to recovered. The "— — —" appear in the DS1 INSERT CHANNEL window indicating that no DS1 signal is being inserted at this time. The **DS1 INSERT CHANNEL** switch should remain in this position until the 310-1 DS1/DS0 Analyzer Option is configured.

3. **PATTERN switch**
   Select INTERNAL DS1 (pattern from the 310-1 DS1/DS0 Analyzer Option).

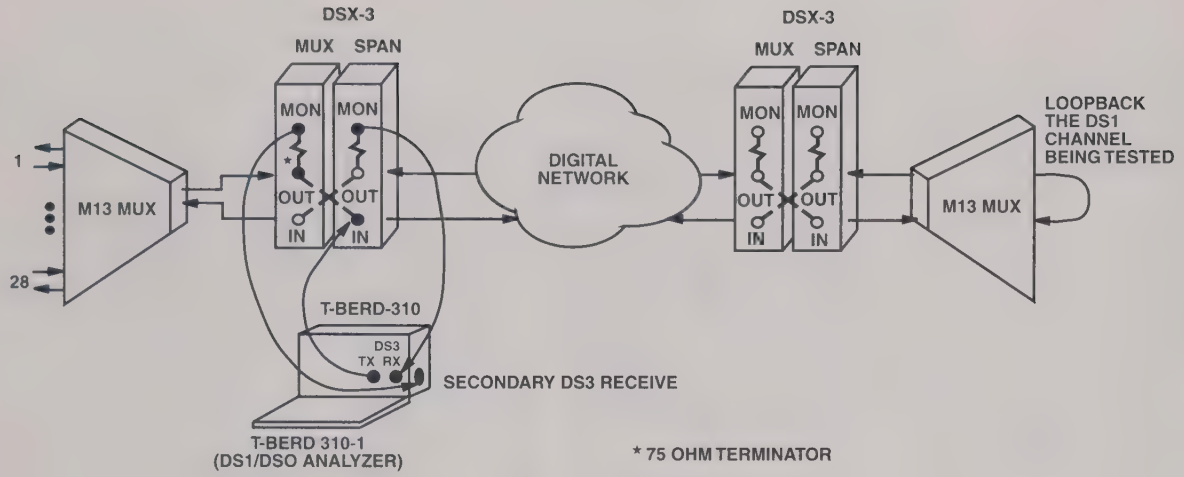


Figure 5-2
Loopback Towards Customer DS1 Signal into a Live DS3 Signal

SECONDARY DS3 RECEIVE jack (side panel)
Plug a cable between this jack and the multiplexer-side MONitor jack. The T-BERD 310 automatically configures itself to the received signal.

RESTART switch
Clear the old results and start a new test.

Secondary DS3 Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, and C-Bit Frame (if applicable).

> If the secondary DS3 signal is not detected (Secondary Signal Present and Secondary Frame Sync LEDs are not illuminated), do not proceed with the need step until the signal and framing are detected.

PRIMARY DS3 TRANSMIT OUTPUT switch and jack
Select the DSX output level and plug a cable between this jack and the span-side IN jack. This should only produce a brief interruption to the DS3 line. Plug the cable into the T-BERD 310 first, then the patch panel to prevent lengthy interruptions.

75 ohm terminator
Plug the terminator into the multiplexer-side OUT jack.

PRIMARY DS3 RECEIVE INPUT switch and jack
Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

RESTART switch
Clear the old results and start a new test.

Primary DS3 Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

12. **RESULTS I and II test results**
    Select the primary SUMMARY category in the RESULTS I window. Select the secondary SUMMARY category in the RESULTS II window. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

310-1 DS1/DS0 Analyzer Option Setup

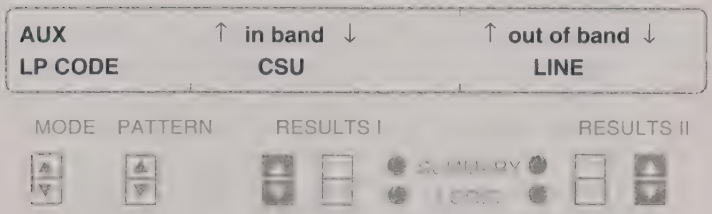
13. **310-1 DS1 SOURCE switch**
    Select DS3 DROP (DS1 dropped from T-BERD 310).

14. **310-1 MODE switch**
    Select an appropriate framing format, e.g., T1 ESF mode.

15. **310-1 PATTERN switch**
    Select an appropriate test pattern, e.g., QRSS.

16. **310-1 TRANSMIT TIMING switch**
    Select INTERNAL.

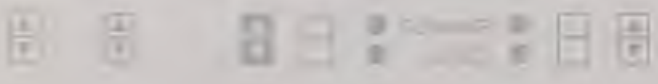
17. **310-1 AUX/PATTERN switches**
    Select the LP CODE auxiliary function to set the in-band or out-of-band loop code.



PATTERN switch (optional)

Select the ESF LOOP auxiliary function to set the ESF loop code type.

AUX	↑	**select**
ESF LOOP		**IN BAND**



AUX switch

Exit the auxiliary functions.

T-BERD 310 Mainframe Setup

DS1 DROP CHANNEL switch

Select the desired DS1 channel to be dropped.

Verify that the Secondary DS2 Frame Sync LED illuminates before continuing with the next step. Inserting the DS1 signal when the LED is not illuminated disrupts the entire DS3 signal.

DS1 INSERT CHANNEL switch

Select the desired DS1 channel of the secondary DS3 received signal that is going to accept the DS1 signal from the 310-1 DS1/DS0 Analyzer Option. As long as the channel number is flashing in the window, the channel can be changed without affecting the DS1 channel. When the channel number stops flashing, the DS1 channel is out-of-service; the other 27 channels are not affected.

310-1 DS1/DS0 Analyzer Option Setup

310-1 LOOP UP switch

Transmit the selected loop-up code. When the loopback is accomplished, the switch LED goes off and the loop code message is replaced with the selected test pattern.

310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

310-1 LOGIC ERROR INSERT switch

Press this switch quickly several times to send logic errors down the circuit. Verify that the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

310-1 RESTART switch

Clear the old results and start a new test.

310-1 RESULTS I test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 LOOP DOWN switch

Transmit the selected loop-down code. When the loopback is released, the switch LED goes off and the loop code message is replaced with the selected test pattern.

Repeat Steps 20 to 28 for the next DS1 channel

Disconnecting the T-BERD 310

Perform the following steps in the indicated order to prevent a disruption of the DS3 signal.

310-1 LOOP DOWN switch

Transmit the selected loop-down code to release the far-end loopback.

DS1 INSERT CHANNEL switch

Display the "— — —" in the DS1 INSERT CHANNEL window.

Unplug the cable from the span-side MONITOR jack (see Figure 5-2)

Unplug the 75 ohm terminator from the multiplexer-side OUT jack

Unplug the cable from the span-side IN jack

Unplug the cable from the multiplexer-side MONITOR jack

T-BERD 310 Results Interpretation

Using the dual DS3 receivers enables T-BERD 310 to verify the DS3 signal quality in both directions before inserting the DS1 channel. Refer to Section 3.2, *Results Interpretation*, to verify that the DS3 signal is error free. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

310-1 Results Interpretation

The insertion of a DS1 test pattern into a live DS3 signal is a means of allowing complete out-of-service DS1 testing from a DS3 access point. Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when performing DS1 insert testing.

5.3 INSERTING AN EXTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

- Access a live DS3 signal and drop and insert a DS1 signal from an external DS1 source (e.g., TTC T-BERD 211).
- Perform an out-of-service loopback test on a DS1 channel of a live DS3 signal.
- Insert an externally generated DS1 test pattern or loop code.
- Perform a bit error rate test on the out-of-service DS1 channel.
- Requires the 310-3 DS1 Insert Option.
- Requires a 75 ohm terminator.

> When this procedure is performed properly, the DS3 signal is unaffected and only one DS1 channel is placed out of service.

Figure 5-3 shows the T-BERD 310 connected to the DSX-3 patch panel. The external DS1 source provides the inserted DS1 channel test pattern and DS1 analysis capabilities.

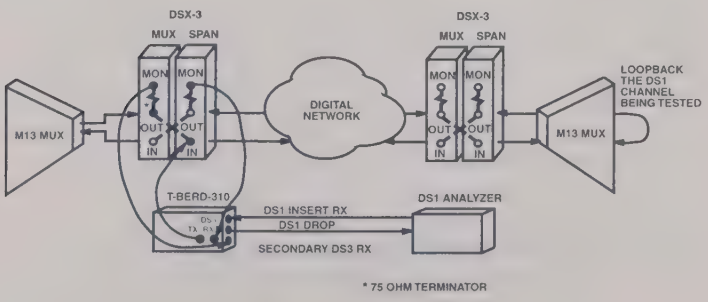


Figure 5-3
Inserting an Externally Generated DS1 Signal Into a Live DS3 Signal

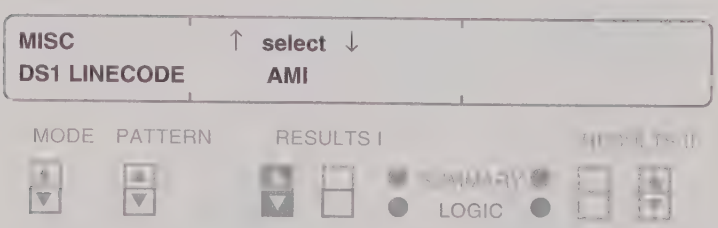
T-BERD 310 Mainframe Setup

DS3 SOURCE switch
Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

MODE switch
Select the DS1 INSERT mode. Transmit timing defaults to recovered. The "— — —" appear in the DS1 INSERT CHANNEL window indicating that no DS1 signal is being inserted at this time. The **DS1 INSERT CHANNEL** switch should remain in this position until the external DS1 source is configured.

PATTERN switch
Select the EXTERNAL DS1 pattern from the DS1 INSERT INPUT jack (side panel).

AUX/MODE/PATTERN switches
Select the DS1 LINECODE auxiliary function to set the transmitted line coding for the DS1 DROP jack (side panel) signal.



5. **AUX switch**
Exit the auxiliary functions.

6. **SECONDARY DS3 RECEIVE jack (side panel)**
Plug a cable between this jack and the multiplexer-side MONitor jack. The T-BERD 310 automatically configures itself to the received signal.

7. **RESTART switch**
Clear the old results and start a new test.

8. **Secondary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, and C-Bit Frame (if applicable).

   NOTE: If the secondary DS3 signal is not detected (Secondary Signal Present and Secondary Frame Sync LEDs are not illuminated), do not proceed with the need step until the signal and framing are detected.

PRIMARY DS3 TRANSMIT OUTPUT switch and jack
Select the DSX output level and plug a cable between this jack and the span-side IN jack. This should only produce a brief interruption to the DS3 line. Plug the cable into the T-BERD 310 first, then the patch panel to prevent lengthy interruptions.

75 ohm terminator
Plug the terminator into the multiplexer-side OUT jack.

PRIMARY DS3 RECEIVE INPUT switch and jack
Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

RESTART switch
Clear the old results and start a new test.

Primary DS3 Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

14. **RESULTS I and II test results**
    Select the primary SUMMARY category in the RESULTS I window. Select the secondary SUMMARY category in the RESULTS II window. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

External DS1 Test Set Setup

Operating mode
Select an appropriately framed DS1 operating mode, e.g., D4, ESF, ESFz, SLC-96, or FT1.

Test pattern
Select an appropriate DS1 test pattern, e.g., QRSS.

Transmit timing
Select INTERNAL.

Configure loop code function
If the DS1 test set has the capability of transmitting and receiving loop codes, configure the test set to transmit and receive the appropriate loop codes.

DS1 test results
Display the appropriate test results.

Receive input termination and connection
Select the TERM input level and connect the DS1 test set receive input connection to the T-BERD 310 DS1 DROP jack (side panel).

Transmit output termination and connection
Select the 0dB(DSX) output level and connect the DS1 test set transmit output connection to the T-BERD 310 DS1 INSERT INPUT jack (side panel).

T-BERD 310 Mainframe Setup

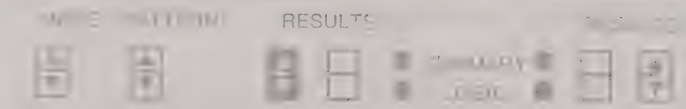
DS1 DROP CHANNEL switch
Select the desired DS1 channel to be dropped through the DS1 DROP jack (side panel) and to the external DS1 test set.

NOTE: Verify that the Secondary DS2 Frame Sync LED is illuminated before continuing with the next step. Inserting the DS1 signal when the LED is not illuminated disrupts the entire DS3 signal.

AUX/MODE/PATTERN switches (optional)

If a SONET drop option is installed, set the DS1 DROP OUT auxiliary function to DS3. This drops the DS1 channel to the DS1 DROP jack (side panel) from the DS3 signal.

SONET	**↑ select ↓**
DS1 DROP OUT	**DS3**



AUX switch

Exit the auxiliary functions.

DS1 INSERT CHANNEL switch

Select the desired DS1 channel of the secondary DS3 received signal that is going to accept the DS1 signal from the DS1 test set. As long as the channel number is flashing in the window, the channel can be changed without affecting the DS1 channel. When the channel number stops flashing the DS1 channel is out-of-service; the other 27 channels are not affected.

External DS1 Test Set Setup

Establish a DS1 channel loopback

Establish a DS1 channel loopback at the far-end of the circuit.

Received signal status

Determine if the external DS1 test set has acquired the received DS1 signal.

Received signal alarm status

Determine if the external DS1 test set has detected any alarmed conditions.

Insert logic errors

Send logic errors down the circuit and verify that the DS1 test set is receiving the proper DS1 signal and errors. This verifies that the transmitted signal is being looped back and received.

Restart the DS1 test set

Clear the old results and start a new test.

DS1 test results

Refer to *External Test Set Results Interpretation* for additional information concerning the results.

Release the DS1 channel loopback

Release the DS1 channel loopback at the far-end of the circuit.

Repeat Steps 22 to 33 for the next DS1 channel

Disconnecting the T-BERD 310

NOTE: Perform the following steps in the indicated order to prevent a disruption of the DS3 signal.

34. **Release the DS1 channel loopback**
Release the DS1 channel loopback at the far-end of the circuit.

35. **DS1 INSERT CHANNEL switch**
Display the "— — —" in the DS1 INSERT CHANNEL window.

36. **Unplug the cable from the span-side MONITOR jack (see Figure 5-3)**

37. **Unplug the 75 ohm terminator from the multiplexer-side OUT jack**

38. **Unplug the cable from the span-side IN jack**

39. **Unplug the cable from the multiplexer-side MONITOR jack**

T-BERD 310 Results Interpretation

Using the dual DS3 receivers enables T-BERD 310 to verify the DS3 signal quality in both directions before inserting the DS1 channel. Refer to Section 3.2, *Results Interpretation*, to verify that the DS3 signal is error free. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

External Test Set Results Interpretation

The insertion of a DS1 test pattern into a live DS3 signal is a means of allowing complete out-of-service DS1 testing from a DS3 access point. Except for BPV results and the receive level result, the results for out-of-service DS1 BERT testing and in-service DS1 monitoring are also applicable when performing DS1 insert testing. Refer to the DS1 test set operating manual for signal analysis capabilities. Full bit error rate testing can be performed on the selected DS1 channel.

DS3 PULSE SHAPE ANALYSIS

In-Service DS3 Pulse Shape Analysis

Out-of-Service DS3 Pulse Shape Analysis

DS3 PULSE SHAPE ANALYSIS

6.1 IN-SERVICE DS3 PULSE SHAPE ANALYSIS

- Monitor the DS3 pulse width, rise time, and fall time on a live circuit.
- Perform DS3 pulse shape analysis at any time while monitoring a live circuit.
- DS3 pulse width, rise time, and fall time can be measured from the DSX-3 MONITOR jack to establish a benchmark of the signal quality while monitoring a live circuit.
- Generate a pulse shape graph showing the pulse shape, width, rise time, and fall time for permanent records.

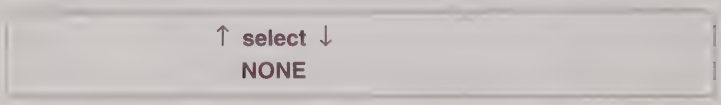
1. **RS-232 graphics-compatible printer (optional)**
   Connect the printer to the RS-232 interface. The printer must be set to accept an 8-bit character format.

2. **DS3 SOURCE switch**
   Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

   NOTE: The DS3 pulse shape analysis can only be performed from the PRIMARY DS3 RECEIVE INPUT jack.

3. **MODE switch**
   Select AUTO.

AUX/MODE/PATTERN switches
Select the PULSE MASK auxiliary function and set to NONE.

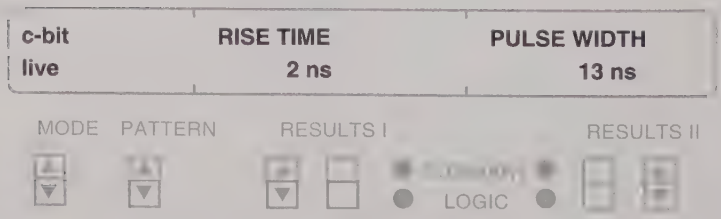


AUX switch
Exit the auxiliary functions.

PRIMARY DS3 RECEIVE INPUT switch and jack
Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

Primary Status LEDs
Verify that the Signal Present LED illuminates.

RESULTS I test results
Select the SIGNAL category and one of the following pulse shape results: PULSE WIDTH, RISE TIME, and FALL TIME. Scroll through the SIGNAL category pulse shape results to determine the pulse shape parameters. Refer to *Results Interpretation* for additional information concerning the results.



9. **AUX/MODE/PATTERN switches (optional)**
Select the GRAPH auxiliary function. Press the **RESULTS I Results** switch to generate the graph. If a printer is not connected, the graph is stored in the print buffer.

PRINT	↑ **print** ↓	
GRAPH	**PULSE**	

10. **AUX switch**
Exit the auxiliary functions.

Results Interpretation

The pulse shape measurements can be made periodically and compared to previous measurements. If a changing trend is noticed, the equipment can be checked and returned to normal before customers notice any problem on the line. The results are recorded in the *results* printouts and the pulse shape graph. When monitoring a DS3 pulse shape, observe the results in the SIGNAL category.

SIGNAL Category

PULSE WIDTH, RISE TIME, and FALL TIME — These results measure the pulse shape in nanoseconds between the 10% and 90% points for the rise time and fall time, and at the 50% points for the pulse width.

NOTE: The PULSE SHAPE result only applies when the PULSE MASK auxiliary function is set to ANSI or CCITT, and the DS3 signal is received from a DSX-3 OUT point. The PULSE MASK auxiliary function setting should be set to NONE to prevent any confusion at seeing a PULSE SHAPE FAIL result.

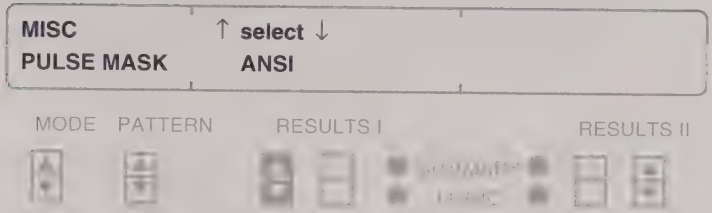
If the pulse shape results display "DENSITY ERR", the signal being monitored does not contain enough isolated pulses to properly measure the pulse shape.

6.2 OUT-OF-SERVICE DS3 PULSE SHAPE ANALYSIS

- Analyze the DS3 pulse shape against the pulse shape mask specified in either the ANSI T1.102-1991 standard or the proposed CCITT G.703 recommendation.
- Measure the DS3 pulse shape from a signal that contains isolated pulses (e.g., 2^23-1 or user-programmed 001 pattern) which is being received at the PRIMARY DS3 RECEIVE INPUT jack and from the DSX-3 level.
- Generate a pulse shape graph showing whether the pulse shape passed or failed against the selected pulse shape mask, pulse width, rise time, and fall time.

1. **Loopback the far end**
   Loopback the far end of the DS3 span at the DSX-3 patch panel.
2. **RS-232 graphics-compatible printer**
   Connect the printer to the RS-232 interface. The printer must be set to accept an 8-bit character format.
3. **DS3 SOURCE switch**
   Select EXT (PRIMARY DS3 RECEIVE INPUT jack).
4. **MODE switch**
   Select an appropriate operating mode, e.g., M13, C-BIT, or UNFRAMED.
5. **PATTERN switch**
   Select a pseudorandom test pattern that generates isolated pulses, e.g., 2^23-1.
6. **TRANSMIT TIMING switch**
   Select INT.

7. **AUX/MODE/PATTERN switches**
   Select the PULSE MASK auxiliary function to set the pulse mask.



8. **AUX switch**
   Exit the auxiliary functions.

9. **PRIMARY DS3 RECEIVE INPUT switch and jack**
   Select the DSX input level and plug a cable between this jack and the span-side OUT jack.

10. **PRIMARY DS3 TRANSMIT OUTPUT switch and jack**
    Select the DSX output level and plug a cable between this jack and the span-side IN jack.

11. **RESTART switch**
    Clear the old results and start a new test.

12. **Primary Status LEDs**
    These LEDs should illuminate: Signal Present, Frame Sync (if applicable), C-Bit Frame (if applicable), and Pattern Sync.

13. **RESULTS I Category switch**
    Select the SUMMARY category.

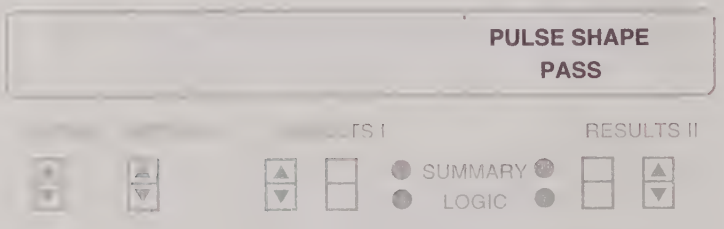
14. **LOGIC ERROR INSERT switch**
    Press this switch quickly several times to send logic errors down the circuit. Verify that the T-BERD 310 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

RESTART switch

Clear the old results and start a new test.

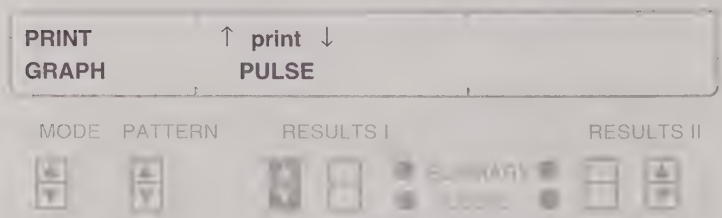
RESULTS II test results

Select SIGNAL category and the PULSE SHAPE result. Refer to *Results Interpretation* for additional information concerning the results.



AUX/MODE/PATTERN switches

Select the GRAPH auxiliary function. Press the **RESULTS I Results** switch to generate the graph. If a printer is not connected, the graph is stored in the print buffer.



AUX switch

Exit the auxiliary functions.

Results Interpretation

The ANSI and CCITT pulse mask specifications are applicable only at the DSX-3 OUT point, and not at the DSX-3 monitor, HIGH, or LOW points. Since testing at the DSX-3 OUT point is an out-of-service test, the PULSE SHAPE PASS/FAIL result provides an easy method to perform equipment verification during installation. When testing a DS3 pulse shape, observe the results in the SIGNAL category.

SIGNAL Category

PULSE WIDTH, RISE TIME, and FALL TIME — These results measure the pulse shape in nanoseconds between the 10% and 90% points for the rise time and fall time, and at the 50% points for the pulse width.

PULSE SHAPE — This result provides a simple PASS/FAIL indication which compares the signal pulse to either the ANSI or CCITT pulse mask specification selected through the PULSE MASK auxiliary function. By selecting a pulse mask, the T-BERD 310 can quickly indicate whether the signal pulses are within the selected pulse mask boundaries.

If the pulse shape results display "DENSITY ERR", the signal being monitored does not contain enough isolated pulses to properly measure the pulse shape.

The pulse shape graph includes the pulse mask, the pulse measurements, power and level readings, and indicates which pulse mask was selected. This hardcopy graph is an excellent tool to visually show that a signal is within specifications or to simplify record keeping.

DS3 JITTER ANALYSIS

Testing for DS3 Wideband and Highband Jitter

DS3 JITTER ANALYSIS

7.1 TESTING FOR DS3 WIDEBAND AND HIGHBAND JITTER

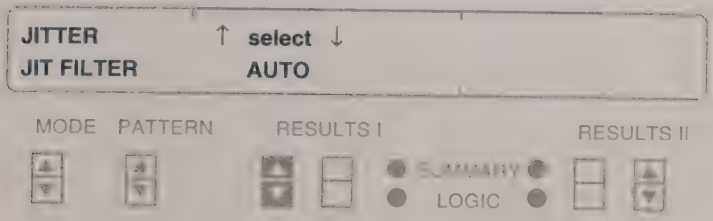
- Test for wideband and highband jitter to determine if it is affecting the DS3 circuit performance.
- Test results provide the current and maximum peak-to-peak wideband (10 Hz to 400 kHz) and highband (30 kHz to 400 kHz) jitter since initial signal presence or test restart. The results are expressed in peak-to-peak Unit Intervals (UIs).
- Demodulated jitter output provides component information to measure the jitter amplitude and frequency with a spectrum analyzer.
- Requires the 310-5 DS3 Jitter Option.

1. **DS3 SOURCE switch**
   Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

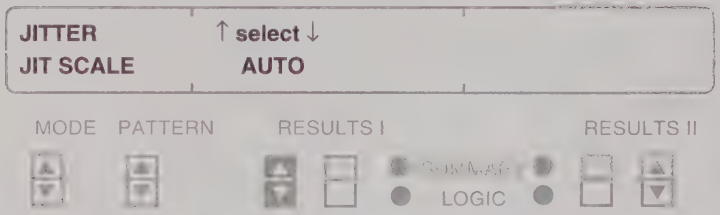
   NOTE The DS3 jitter analysis can only be performed from the PRIMARY DS3 RECEIVE INPUT jack.

2. **MODE switch**
   Select AUTO.

3. **AUX/MODE/PATTERN switches**
   Select the JIT FILTER auxiliary function to set the filter bandwidth.



4. **PATTERN switch**
   Select the JIT SCALE auxiliary function to set the jitter amplitude scale.



5. **AUX switch**
   Exit the auxiliary functions.

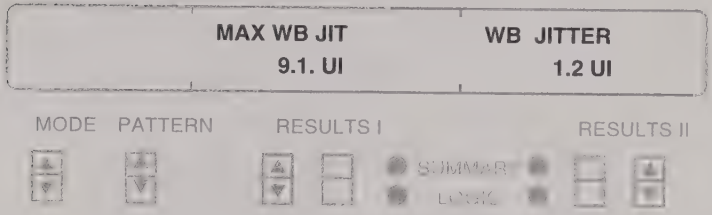
6. **PRIMARY DS3 RECEIVE INPUT switch and jack**
   Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

7. **RESTART switch**
   Clear the old results and start a new test.

8. **Primary Status LEDs**
   Verify that the Signal Present LED illuminates.

9. **RESULTS I and II test results**
   Select the SIGNAL category and the jitter results. Select the MAX WB JIT and WB JITTER to measure the wideband jitter. Select the MAX HB JIT and HB JITTER to measure the highband jitter. If the AUTO mode is selected in the jitter

auxiliary functions, the associated results provide the necessary measurements that coincide with the selected filter and scale. Refer to *Results Interpretation* for additional information concerning the results.



10. **JITTER OUTPUT jack (side panel)**
Connect a spectrum analyzer to this jack. Determine the jitter amplitudes and frequencies.

Results Interpretation

The DS3 jitter measurements allow sources of jitter to be identified. When monitoring a DS3 signal for jitter, observe the results in the SIGNAL category.

SIGNAL Category

WB JITTER and MAX WB JIT — The wideband frequency bandwidth is 10 Hz to 400 kHz. Measure the wideband and maximum wideband jitter first. If unacceptable jitter is present, measure the highband and maximum highband jitter.

HB JITTER, and MAX HB JIT — The highband frequency bandwidth is 30 kHz to 400 kHz. If excess jitter is present in the highband results, the jitter could be caused by a number of accumulating sources such as along a regenerator span. If the highband readings do not indicate excess jitter, then the jitter is present in the lowband region (10 Hz to 30 kHz). Lowband jitter is usually caused by a single piece of equipment such as an M13 multiplexer.

DS3 MULTIPLEXER TESTING

M13 Multiplexer (Multiplex Test)

M13 Multiplexer (Demultiplex Test)

M13 Multiplexer (Multiplex/Demultiplex Test)

DS3 MULTIPLEXER TESTING

8.1 M13 MULTIPLEXER (MULTIPLEX TEST)

- Verify the multiplexing functionality from the low-speed DS1 input to the high-speed DS3 output of a M13 multiplexer.
- Transmit a DS1 test pattern into each of the M13 multiplexer low-speed inputs.
- Perform DS3 testing on the M13 multiplexer output.
- Drop each DS1 channel from the DS3 signal and perform complete bit error rate analysis.
- Requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-1 shows the T-BERD 310 connected to the low-speed DS1 channel input and the high-speed DS3 output of the M13 multiplexer.

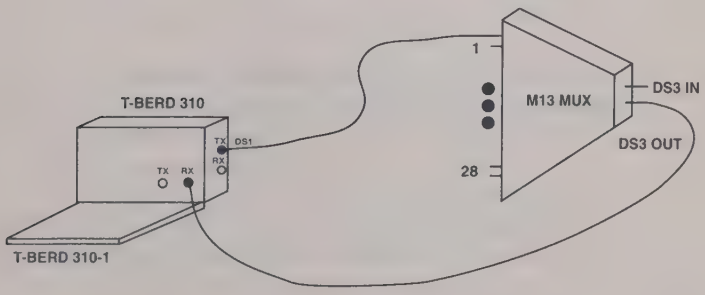


Figure 8-1
Testing the Multiplexing Capability of a DS3 Multiplexer

310-1 DS1/DS0 Analyzer Option Setup

310-1 MODE switch
Select an appropriate framing format, e.g., T1 ESF mode.

310-1 PATTERN switch
Select an appropriate test pattern, e.g., QRSS.

310-1 TRANSMIT TIMING switch
Select INTERNAL.

310-1 CODE switch
Select AMI or B8ZS encoding.

310-1 DS1 TRANSMIT jack (side panel)
Plug a cable between this jack and one of the low-speed DS1 inputs of the DS3 multiplexer.

T-BERD 310 Mainframe Setup

DS3 SOURCE switch
Select EXT (PRIMARY DS3 RECEIVE INPUT jack).

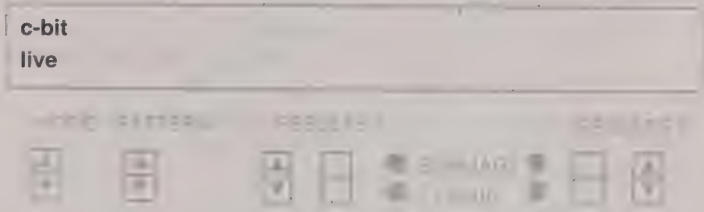
7. **MODE switch**
Select AUTO.

8. **PRIMARY DS3 RECEIVE INPUT switch and jack**
Select the HIGH input level and plug a cable between this jack and the high-speed DS3 output of the DS3 multiplexer.

9. **Primary Status LEDs**
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

MODE/PATTERN window

Verify the framing format and pattern.



RESULTS I test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

DS1 DROP CHANNEL switch

Select the DS1 channel being dropped from the DS3 signal to the 310-1 DS1/DS0 Analyzer Option.

310-1 DS1/DS0 Analyzer Option Setup

310-1 DS1 SOURCE switch

Select DS3 DROP (DS1 dropped from T-BERD 310).

310-1 RESTART switch

Clear the old results and start a new test.

310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

16. **310-1 RESULTS I Category switch**
Select the SUMMARY category.

17. **310-1 LOGIC ERROR INSERT switch**
Press this switch quickly several times to send logic errors down the circuit. Verify that the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

18. **310-1 RESTART switch**
Clear the old results and start a new test.

19. **310-1 RESULTS II test results**
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

Testing the Next DS1 Channel

20. **310-1 DS1 TRANSMIT jack (side panel)**
Plug the cable between this jack and the next low-speed DS1 input of the DS3 multiplexer.

21. **T-BERD 310 DS1 DROP CHANNEL switch**
Select the next DS1 channel being dropped from the DS3 signal to the 310-1 DS1/DS0 Analyzer Option.

22. **310-1 RESTART switch**
Clear the old results and start a new test.

23. **310-1 Status LEDs**
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

24. **310-1 RESULTS II test results**
Refer to *310-1 Results Interpretation* for additional information concerning the results.

25. **Test the next low-speed DS1 channel**
Repeat Steps 20 through 25 to test all of the low-speed DS1 channels.

T-BERD 310 Results Interpretation

When monitoring the DS3 signal, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories. Refer to Section 3.1 *Results Interpretation* to verify that the DS3 signal is error free. Note that the DS3 LOGIC category results are not applicable since the received signal contains multiplexed DS1 patterns and NOT a DS3 test pattern. Once the DS3 results are verified, the DS1 channel can be tested.

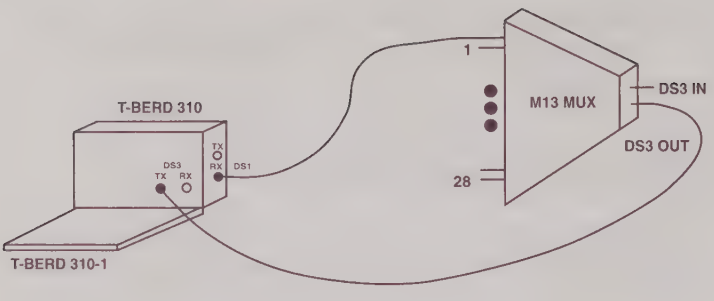
310-1 Results Interpretation

Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the selected DS1 channel. When performing the test, observe the results in the LOGIC, FRAME, and SIGNAL categories.

8.2 M13 MULTIPLEXER (DEMULTIPLEX TEST)

- Verify the demultiplexing functionality from the high-speed DS3 input to the low-speed DS1 output of a M13 multiplexer.
- Transmit a multiplexed DS3 signal into the M13 multiplexer high-speed input.
- Perform complete bit error rate testing on each of the DS1 signals demultiplexed by the M13 multiplexer.
- Requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-2 shows the T-BERD 310 connected to the low-speed DS1 channel output and the high-speed DS3 input of the M13 multiplexer.



T-BERD 310 Mainframe Setup

MODE switch

Select an appropriate channelized framing format, e.g., MUXED M13 or MUXED C-BIT mode. The "— — —" appear in the DS1 INSERT CHANNEL window indicating that an All Ones pattern is being inserted at this time.

PATTERN switch

Select an appropriate channelized DS1 test pattern, e.g., T1D4 QRSS.

TRANSMIT TIMING switch

Select INT.

PRIMARY DS3 TRANSMIT OUTPUT switch and jack

Select the LOW output level and plug a cable between this jack and the high-speed DS3 input of the M13 multiplexer.

310-1 DS1/DS0 Analyzer Option Setup

310-1 DS1 SOURCE switch
Select EXT INPUT.

310-1 MODE switch
Select AUTO.

310-1 RECEIVE INPUT switch and DS1 RECEIVE jack (side panel)
Select the TERM input level and plug a cable between this jack and the DS1 channel output being tested.

T-BERD 310 Mainframe Setup

DS1 INSERT CHANNEL switch
Select the DS1 channel being tested. The selected DS1 channel contains the selected test pattern (see Step 2). The other DS1 channels contain an All Ones pattern.

DS1 DROP CHANNEL switch
Select the DS1 channel being tested.

310-1 DS1/DS0 Analyzer Option Setup

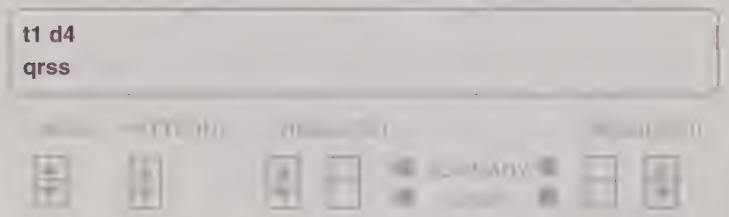
310-1 RESTART switch
Clear the old results and start a new test.

310-1 Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

310-1 Alarm LEDs
These LEDs should not be illuminated. If the All Ones LED illuminates, verify that the T-BERD 310 is connected properly and the **DS1 DROP CHANNEL** and **DS1 INSERT CHANNEL** switches are set properly.

310-1 MODE/PATTERN window

Verify the framing format and pattern. The framing format and test pattern must match the framing format and test pattern selected in Step 2.



310-1 RESULTS I test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

Test the next low-speed DS1 channel

Repeat Steps 7 through 15 to test the other low-speed DS1 channels.

310-1 Results Interpretation

All DS1 results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the demultiplexing functionality. When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories.

Testing the demultiplexing functionality of an M13 multiplexer involves transmitting a multiplexed DS3 test signal into the multiplexer DS3 input. The transmitted DS3 test signal (MUXED M13 or MUXED C-BIT) contains 28 multiplexed DS1 test patterns and the proper DS1, DS2, and DS3 framing and overhead bits to allow the multiplexer to receive and demultiplex the DS3 test signal into the 28 DS1 channels.

The selected DS1 test pattern can be inserted into ALL 28 DS1 channels, or into only one selected DS1 channel with the remaining 27 DS1 channels containing an ALL ONES pattern. Inserting the DS1 pattern into only one DS1 channel allows each DS1 to be isolated and verification that the multiplexer is demultiplexing each DS1 to the proper DS1 output.

8.3 M13 MULTIPLEXER (MULTIPLEX/DEMULTIPLEX TEST)

- Perform bit error rate test between the low-speed DS1 ends of a DS3 network.
- Verify the multiplexing/demultiplexing functionality of the M13 multiplexers.
- Requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-3 shows the T-BERD 310 connected to the near-end low-speed DS1 side of a M13 multiplexer and the far-end low-speed DS1 side looped back.

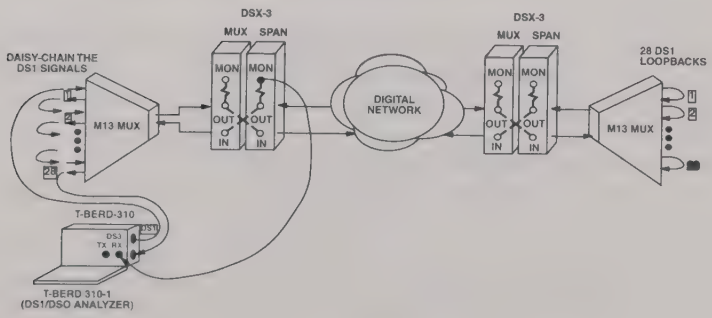


Figure 8-3
Testing the DS3 Multiplexing/Demultiplexing Capability

Network Configuration

Daisy chain the near-end DS1 channels
Connect the output of Channel 1 to the input of Channel 2, the output of Channel 2 to the input of Channel 3, etc. The input for Channel 1 and the output for Channel 28 should be open.

Loopback the far-end DS1 channels
Loopback all 28 DS1 channels manually, with cables.

310-1 DS1/DS0 Analyzer Option Setup

310-1 DS1 SOURCE switch
Select EXT. INPUT (side-panel DS1 RECEIVE jack).

310-1 MODE switch
Select an appropriate framing format, e.g., T1 D4.

310-1 PATTERN switch
Select an appropriate test pattern, e.g., QRSS.

310-1 TRANSMIT TIMING switch
Select INTERNAL.

310-1 CODE switch
Select AMI or B8ZS encoding.

310-1 RECEIVE INPUT switch and DS1 RECEIVE jack (side panel)
Select the TERM input level and plug a cable between this jack and the low-speed output for DS1 channel 28.

310-1 DS1 TRANSMIT jack (side panel)
Plug a cable between this jack and the low-speed input for DS1 channel 1.

310-1 RESTART switch
Clear the old results and start a new test.

310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, Pattern Sync, and B8ZS (if applicable).

310-1 RESULTS I Category switch

Select the SUMMARY category.

310-1 LOGIC ERROR INSERT switch

Press this switch quickly several times to send logic errors down the circuit. Verify that the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies that the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

310-1 RESTART switch

Clear the old results and start a new test.

310-1 RESULTS II test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 Results Interpretation

All DS1 results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the multiplexing/demultiplexing functionality of the network. When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories. This application allows multiplexing and demultiplexing testing of each M13 multiplexer while also testing the integrity of the full end-to-end transmission path using only a single DS1 transmitter and receiver.

DIGITAL CROSS-CONNECT TESTING

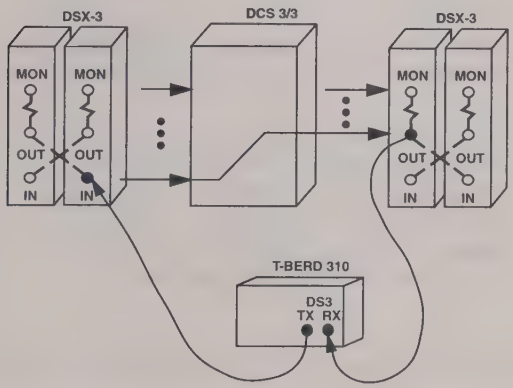
DCS 3/3 Testing

DCS 3/1 Testing

9.1 DCS 3/3 TESTING

- Verify the DCS 3/3 cross-connect mapping.

Figure 9-1 illustrates the test setup with the T-BERD 310 connected to the DCS 3/3.



MODE switch

Select M13 or C-BIT mode.

PATTERN switch

Select a nonchannelized DS3 test pattern, e.g., 2^23-1.

TRANSMIT TIMING switch
Select INT.

PRIMARY DS3 RECEIVE INPUT switch and jack
Select the DSX input level and plug a cable between this jack and the DS3 East-side OUT jack.

PRIMARY DS3 TRANSMIT OUTPUT switch and jack
Select the DSX (LOW for < 200 feet) output level and plug a cable between this jack and the DS3 West-side IN jack.

310-1 RESTART switch
Clear the old results and start a new test.

Primary Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, Pattern Sync, and C-Bit Frame (if applicable).

8. **RESULTS I test results**
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

Results Interpretation

The DS3 test pattern is transmitted into a DCS DS3 input, and received through the mapped DCS DS3 output to the T-BERD 310. If the DS3 signal is mapped correctly through the DCS 3/3, the T-BERD 310 indicates frame and pattern synchronization. The results for out-of-service DS3 BERT testing (see Section 4.1) and in-service DS3 monitoring (see Section 3.1) are applicable when testing the DCS DS3 signal. When performing the test, observe the results in the LOGIC, BPV, PARITY, FRAME, and SIGNAL categories.

9.2 DCS 3/1 TESTING

- Verify the DCS 3/1 cross-connect mapping.
- Requires the 310-1 DS1/DS0 Analyzer Option.

Figure 9-2 illustrates the test setup with the T-BERD 310 connected to the DCS 3/1.

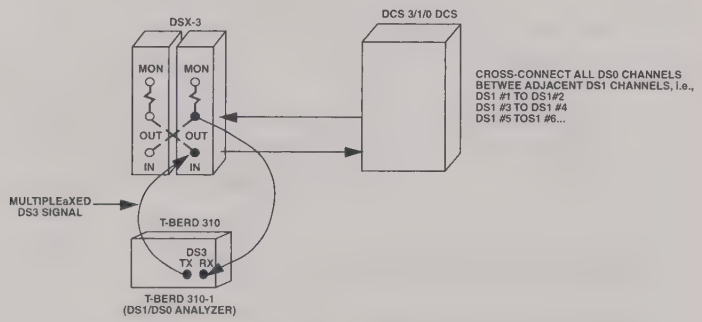


Figure 9-2
Setting Up for DCS 3/1 Testing

T-BERD 310 Mainframe Setup

1. **MODE switch**
   Select the MUXED M13 or MUXED C-BIT mode. The "— — —" appear in the DS1 INSERT CHANNEL window indicating that an All Ones pattern is being inserted at this time.

2. **PATTERN switch**
   Select a channelized DS1 test pattern, e.g., T1D4 QRSS.

3. **TRANSMIT TIMING switch**
   Select INT.

4. **PRIMARY DS3 RECEIVE INPUT switch and jack**
   Select the DSX input level and plug a cable between this jack and the DS3 East-side OUT jack.

PRIMARY DS3 TRANSMIT OUTPUT switch and jack
Select the DSX output level and plug a cable between this jack and the DS3 West-side IN jack.

RESTART switch
Clear the old results and start a new test.

Primary Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

310-1 DS1/DS0 Analyzer Option Setup

310-1 DS1 SOURCE switch
Select DS3 DROP (DS1 dropped from T-BERD 310).

310-1 MODE switch
Select AUTO.

Verifying the DS1 Channel Mapping

DS1 INSERT CHANNEL switch
Insert the test pattern into the first mapped DS1 channel.

DS1 DROP CHANNEL switch
Drop the first mapped DS1 channel.

310-1 RESTART switch
Clear the old results and start a new test.

310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

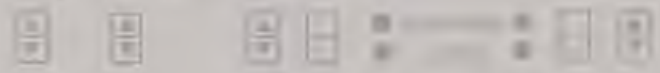
310-1 Alarm LEDs

These LEDs should not be illuminated. If the All Ones LED illuminates, check the DS1 mapping and the selected channels.

310-1 MODE/PATTERN window

Verify the framing format and pattern. The indicated framing format and pattern should match the framing format and pattern selected in Step 2, e.g., T1D4 QRSS.

t1 d4	ALL	BIT ERRORS
qrss	RESULTS OK	0



310-1 RESULTS I test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

Repeat Steps 11 to 18 to verify the next mapped DS1 channel

T-BERD 310 Results Interpretation

Testing the DCS 3/1 mapping involves transmitting a multiplexed DS3 test signal into the DCS DS3 input. The transmitted DS3 test signal (MUXED M13 or MUXED C-BIT) contains 28 multiplexed DS1 test patterns and the proper DS1, DS2, and DS3 framing and overhead bits to allow the DCS 3/1 to receive and redirect the DS1 channels into the appropriately mapped DS3 output. The T-BERD 310 receives the DS3 output and drops the DS1 test pattern to the 310-1 DS1/DS0 Analyzer Option.

If the DCS DS3 signals have been mapped correctly, the T-BERD 310 indicates DS3 frame synchronization (Frame Sync LED illuminates).

310-1 Results Interpretation

Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when verifying the DCS 3/1 mapping. When performing an out-of-service DS1 bit error rate test from a DS3 access point, observe the results in the LOGIC, FRAME, and SIGNAL categories.

The selected DS1 test pattern can be inserted into ALL 28 DS1 channels, or into only one selected DS1 channel with the remaining 27 DS1 channels containing an ALL ONES pattern. Inserting the DS1 pattern into only one DS1 channel allows each DS1 to be isolated and verified that the DCS 3/1 is mapping each DS1 channel from the proper DS3 input and to the proper DS3 output.

If the DCS DS1 signals have been mapped correctly, the T-BERD 310-1 indicates DS1 frame and pattern synchronization to the DS1 signal (Frame Sync LED and Pattern Sync LED illuminate).

SONET TESTING

Monitoring STS-1 or OC-n Signals and DS3 or DS1 Payloads

Testing Low-Speed (DS3/DS1) to High-Speed (SONET) Circuits

Testing High-Speed (SONET) to Low-Speed (DS3/DS1) Circuits

SONET TESTING

10.1 MONITORING STS-1 OR OC-N SIGNALS AND DS3 OR DS1 PAYLOADS

- Evaluate the SONET STS-1 or OC-n (n is 1, 3, or 12) performance while dropping and analyzing a DS3 or DS1 payload from the SONET signal.
- Requires the 310-1 and either the 310-4, 310-4A, 310-12, 310-13R, or 310-14R option.

Figure 10-1 illustrates how the T-BERD 310 connects to the SONET circuit to analyze SONET overhead and a DS3 or DS1 payload. The following application is divided into three parts:

- T-BERD 310 SONET Receiver Setup and Analysis
- T-BERD 310 DS3 Receiver Setup and Analysis
- 310-1 DS1 Receiver Setup and Analysis

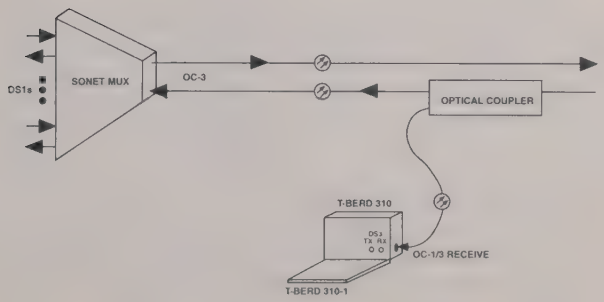


Figure 10-1
Setup for Monitoring SONET Signals and a DS3 or DS1 Payload from a SONET Access Point

T-BERD 310 SONET Receiver Setup and Analysis

1. **AUX/MODE switches**
   Select the SONET RX auxiliary group.

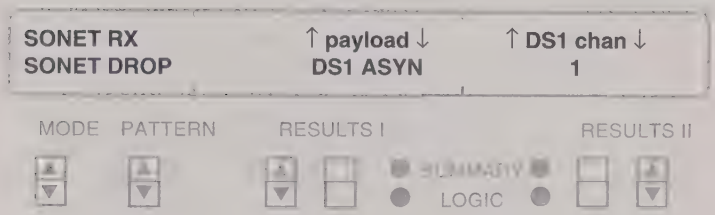
2. **PATTERN/RESULTS switches**
   Select the SONET INPUT auxiliary function and the desired side-panel SONET input as indicated below (step does not apply to the 310-4 or 310-13R):

SONET RX SONET INPUT	↑ select ↓ OC-3	↑ STS ID ↓ 2

SONET INPUT Auxiliary Function			
Selection	**STS ID**	**Connector**	**Option**
STS-1	—	STS-1 RECEIVE	310-4A 310-14R
OC-1	—	OC-1/OC-3 RECEIVE	310-4A 310-14R
OC-3	1 to 3	OC-1/OC-3 RECEIVE	310-4A 310-14R
OC-12	1 to 12	OC-12 RECEIVE	310-12

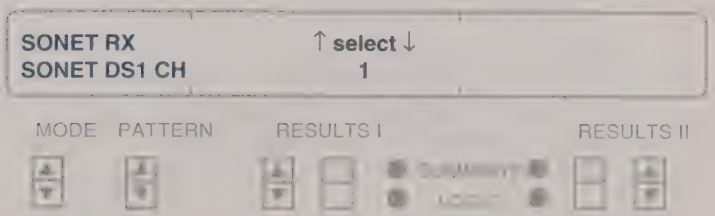
3. **PATTERN/RESULTS switch**

For the 310-12, 310-13R, and 310-14R options, select the SONET DROP auxiliary function and the desired payload or AUTO as indicated below:



SONET DROP Auxiliary Function					
Payload	**AUTO**	**DS3 ASYN**	**DS1 ASYN**	**DS1 BIT**	**DS1 BYTE**
DS1 Channel	N/A DS3/ 1 to 28 DS1	—	1 to 28	1 to 28	1 to 28
Drop To	310/310-1	310	310-1	310-1	310-1

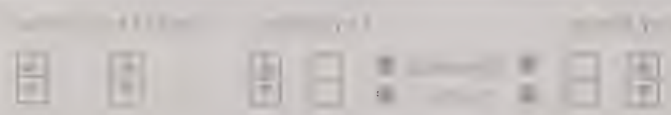
For the 310-4 and 310-4A options, select the SONET DS1 CH auxiliary function and DS1 channel (1 to 28) to be dropped from a SONET DS1 signal with either DS1 asynchronous or DS1 bit synchronous mapping.



5. **PATTERN/RESULTS switch**

   If testing an STS-1 signal, select the STS RX LEVEL auxiliary function and set the STS-1 signal input level.

SONET RX	**↑ select ↓**
STS RX LEVEL	**DSX**



6. **AUX switch**

   Exit the auxiliary functions.

8. **SONET connections**

   Connect a SONET cable to the desired connection:

   - STS-1 RECEIVE
   - OC-1/OC-3 RECEIVE
   - OC-12 RECEIVE

   NOTE Clean optical connections with denatured alcohol before attaching them to the T-BERD 310 optical connectors.

7. **RESTART switch**

   Clear the old results and start new test.

8. **Status LEDs**

   The SONET Present LED should illuminate indicating a valid framed SONET signal. For optical inputs on the 310-12 and 310-14R options, verify that the side-panel LED above either the OC-1/OC-3 RECEIVE or OC-12 RECEIVE optical connector illuminates when the cable is connected indicating a signal is present.

RESULTS I test results

Select the SUMMARY category. If no errors are detected in the SONET overhead, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *SONET Results Interpretation* for additional information concerning the results. SONET ALARMS appear in the SUMMARY category as follows:

LOS	Loss of Signal alarm
LOF	Loss of Frame alarm
SEF	Severely Errored Frame alarm
LINE AIS	Line alarm indication signal (AIS) alarm
LINE RDI	Line remote defect indication (RDI) alarm
PATH AIS	Path AIS alarm
PATH RDI	Path RDI alarm (also known as RAI or Yellow Alarm)
PATH LOP	Path loss of pointer (LOP) alarm
VT AIS	VT AIS alarm
VT RDI	VT RDI alarm (also known as RAI or Yellow Alarm)
VT LOP	VT LOP alarm

SONET Results Interpretation

The T-BERD 310 can monitor the SONET signal overhead information and present the results in the SONET category.

Section, Line, Path, VT, and Equivalent Bit Error Rate BIP results — Bit interleave parity errors indicate that data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

FRM WORD ERR and SON SEF SEC — Frame Word Errors and SONET Severely Errored Frame Seconds indicate that incorrect framing bits are being generated by the SONET equipment or corrupted during transmission.

POINTER JUST, POINTER INC, POINTER DEC, POINTER NDF, and POINTER DATA — Line pointer justification results monitor for excessive changes in the SPE payload pointer, which could indicate a network timing problem between SONET nodes.

APS MSG CNT, APS INFO, and APS CONFIG — Automatic protection switching results indicate the number of APS messages that have been received, the last APS message received, and the APS configuration.

SONET RX FREQ — The SONET received frequency measurement verifies the received SONET signal frequency in Hertz.

T-BERD 310 DS3 Receiver Setup and Analysis

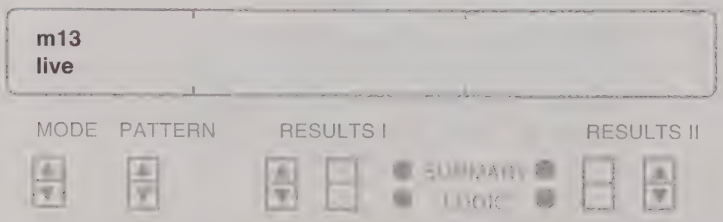
1. **DS3 SOURCE switch**
   Select SONET.

2. **MODE switch**
   Select AUTO.

3. **RESTART switch**
   Clear the old results and start new test.

4. **Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

5. **310 MODE/PATTERN window**
   Verify the framing format and pattern.



6. **RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the DS3 payload, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

7. **DS1 DROP CHANNEL switch (optional)**
   If the DS3 signal is properly framed (DS2 and DS1 framing), DS1 or E1 channels can be dropped and monitored. The DS1 channels can be dropped to either the 310-1 DS1/DS0 Analyzer Option or DS1 DROP jack (side panel) and an external DS1 test set. The E1 channels can be dropped to the E1 DROP jack (side panel) and an external E1 test set.

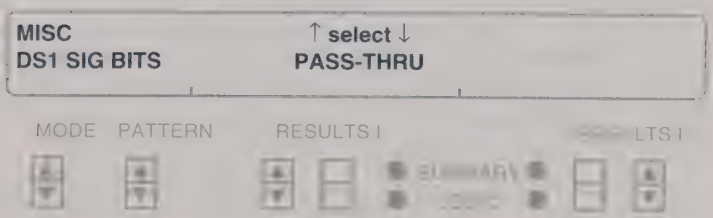
T-BERD 310 Results Interpretation

Except for the BPV category, level, power, pulse shape, and jitter results (since the DS3 signal is internally dropped from the SONET signal), the other results for in-service DS3 monitoring (see Section 3.1) are applicable when testing a DS3 signal dropped from a SONET signal.

310-1 DS1 Receiver Setup and Analysis

1. **310-1 DS1 SOURCE switch**
   Select SONET DROP.

2. **T-BERD 310 AUX/MODE/PATTERN/RESULTS switches**
   Select the MISC auxiliary group, DS1 SIG BITS auxiliary function, and set the DS1 signaling transfer mode.



310-1 MODE switch
Select AUTO.

310-1 RESTART switch
Clear the old results and start a new test.

310-1 Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

310-1 MODE/PATTERN window
Verify the framing format and pattern.

310-1 RESULTS I test results
Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 Results Interpretation

When monitoring a DS1 payload from a SONET signal, observe the results in the FRAME and SIGNAL categories.

NOTE The BPV category and RX LVL dBdsx result are not applicable since the DS1 channel is dropped internally from within a SONET signal.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

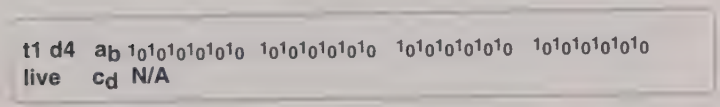
SIGNAL Category

The SIGNAL category results include both DS1 and DS0 measurements.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification, the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.



10.2 TESTING LOW-SPEED (DS3/DS1) TO HIGH-SPEED (SONET) CIRCUITS

- Test SONET multiplexer (SM), add/drop multiplexer (ADM), or digital cross-connect system (DCS) circuit functionality from the low-speed DS1 or DS3 side to the high-speed SONET STS-1 or OC-n (n is 1, 3, or 12) side while dropping and analyzing the DS3 or DS1 payload from the SONET signal.

- Requires the 310-1 and either the 310-4, 310-4A, 310-12, 310-13R, or 310-14R option.

Figure 10-2 illustrates how the T-BERD 310 connects to the SONET circuit to analyze SONET overhead and a DS3 or DS1 payload. The following application is divided into five parts:

- T-BERD 310 SONET Receiver Setup and Analysis
- T-BERD 310 DS3 Transmitter Setup
- 310-1 DS1 Transmitter Setup
- T-BERD 310 DS3 Receiver Setup and Analysis
- 310-1 DS1 Receiver Setup and Analysis

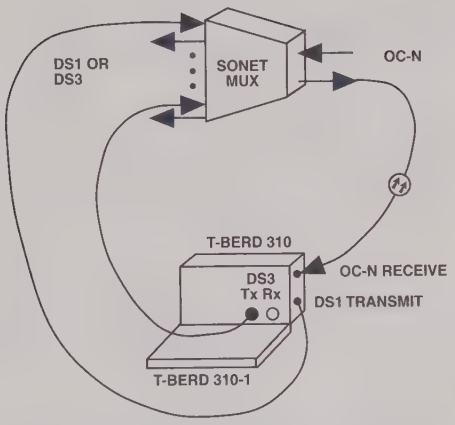


Figure 10-2
Setup for Testing Low- to High-Speed SONET Circuits

T-BERD 310 SONET Receiver Setup

AUX/MODE switches

Select the SONET RX auxiliary group.

PATTERN/RESULTS switches

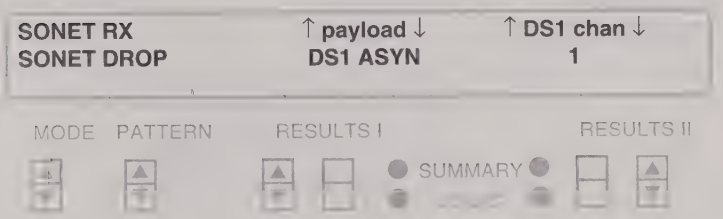
Select the SONET INPUT auxiliary function and the desired side-panel SONET input as indicated below (step does not apply to the 310-4 or 310-13R):

SONET RX SONET INPUT	**↑ select ↓ OC-3**	**↑ STS ID ↓ 2**

SONET INPUT Auxiliary Function			
Selection	**STS ID**	**Connector**	**Option**
STS-1	—	STS-1 RECEIVE	310-4A 310-14R
OC-1	—	OC-1/OC-3 RECEIVE	310-4A 310-14R
OC-3	1 to 3	OC-1/OC-3 RECEIVE	310-4A 310-14R
OC-12	1 to 12	OC-12 RECEIVE	310-12

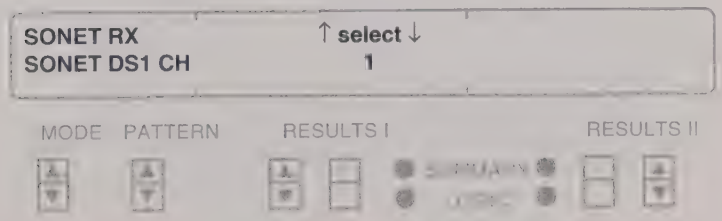
PATTERN/RESULTS switch

For the 310-12, 310-13R, and 310-14R options, select the SONET DROP auxiliary function and the desired payload or AUTO as indicated below:

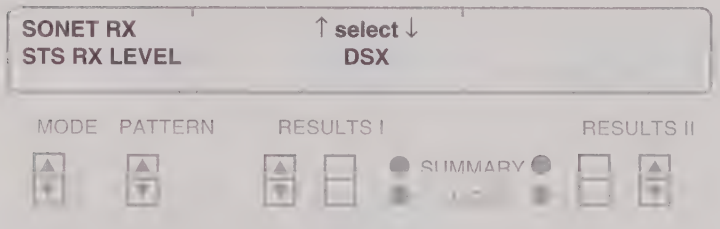


SONET DROP Auxiliary Function					
Payload	**AUTO**	**DS3 ASYN**	**DS1 ASYN**	**DS1 BIT**	**DS1 BYTE**
DS1 Channel	N/A DS3 / 1 to 28 DS1	—	1 to 28	1 to 28	1 to 28
Drop To	310 / 310-1	310	310-1	310-1	310-1

For the 310-4 and 310-4A options, select the SONET DS1 CH auxiliary function and DS1 channel (1 to 28) to be dropped from a SONET DS1 signal with either DS1 asynchronous or DS1 bit synchronous mapping.



4. **PATTERN/RESULTS switch**
   If testing an STS-1 signal, select the STS RX LEVEL auxiliary function and set the STS-1 signal input level.



5. **AUX switch**
   Exit the auxiliary functions.

6. **SONET connections**
   Connect a SONET cable to the desired connection:

   - STS-1 RECEIVE
   - OC-1/OC-3 RECEIVE
   - OC-12 RECEIVE

   NOTE: Clean optical connections with denatured alcohol before attaching them to the T-BERD 310.

T-BERD 310 DS3 Transmitter Setup

1. **MODE switch**
   Select appropriate framing mode, e.g., to test a non-channelized DS3 signal select M13 or C-BIT, to test a channelized DS3 signal select MUXED C-BIT or MUXED M13.

2. **PATTERN switch**
   Select appropriate test pattern, e.g., to test a non-channelized DS3 signal select 2^23-1, 2^20-1, etc., to test a channelized DS3 signal select T1ESF QRSS, T1D4 QRSS, etc.

3. **TRANSMIT TIMING switch**
   Select INT.

4. **PRIMARY DS3 TRANSMIT OUTPUT switch and jack**
   Select LOW output level and plug a cable between this jack and the low-speed DS3 input of the SONET multiplexer or add/drop multiplexer.

T-BERD 310-1 DS1 Transmitter Setup

1. **310-1 MODE switch**
   Select appropriate framing mode, e.g., T1 D4 or T1 ESF.

2. **310-1 PATTERN switch**
   Select appropriate DS1 test pattern, e.g., QRSS.

3. **310-1 TRANSMIT TIMING switch**
   Select INTERNAL.

4. **310-1 CODE switch**
   Select either AMI or B8ZS.

5. **310-1 DS1 TRANSMIT jack (side panel)**
   Plug a cable between this jack and the low-speed DS1 input of the SONET multiplexer or add/drop multiplexer.

T-BERD 310 SONET Received Signal Analysis

1. **RESTART switch**
   Clear the old results and start new test.

2. **Status LEDs**
   The SONET Present LED should illuminate indicating a valid framed SONET signal. For optical inputs on the 310-12 and 310-14R options, verify that the side-panel LED above either the OC-1/OC-3 RECEIVE or OC-12 RECEIVE optical connector illuminates when the cable is connected indicating a signal is present.

RESULTS I test results

Select the SUMMARY category. If no errors are detected in the SONET overhead, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *SONET Results Interpretation* for additional information concerning the results. SONET ALARMS appear in the SUMMARY category as follows:

LOS	Loss of Signal alarm
LOF	Loss of Frame alarm
SEF	Severely Errored Frame alarm
LINE RDI	Line remote defect indication (RDI) alarm
PATH AIS	Path AIS alarm
PATH RDI	Path RDI alarm (also known as RAI or Yellow Alarm)
PATH LOP	Path loss of pointer (LOP) alarm
VT AIS	VT AIS alarm
VT RDI	VT RDI alarm (also known as RAI or Yellow Alarm)
VT LOP	VT LOP alarm

SONET Results Interpretation

The T-BERD 310 can monitor the SONET signal overhead and present the results in the SONET category.

Section, Line, Path, VT, and Equivalent Bit Error Rate BIP results — Bit interleave parity errors indicate that data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

FRM WORD ERR and SON SEF SEC — Frame Word Errors and SONET Severely Errored Frame Seconds indicate that incorrect framing bits are being generated by the SONET equipment or corrupted during transmission.

POINTER JUST, POINTER INC, POINTER DEC, POINTER NDF, and POINTER DATA — Line pointer justification results monitor for excessive changes in the SPE payload pointer, which could indicate a network timing problem between SONET nodes.

APS MSG CNT, APS INFO, and APS CONFIG — Automatic protection switching results indicate the number of APS messages that have been received, the last APS message received, and the APS configuration.

SONET RX FREQ — The SONET received frequency measurement verifies the received SONET signal frequency in Hertz.

T-BERD 310 DS3 Receiver Setup and Analysis

DS3 SOURCE switch
Select SONET.

RESTART switch
Clear the old results and start new test.

Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

RESULTS I test results
Select the SUMMARY category. If no errors are detected in the DS3 payload, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

DS1 DROP CHANNEL switch (optional)
If the DS3 signal is properly framed for MUXED M13 or MUXED C-BIT, DS1 channels can be dropped and monitored by the 310-1 DS1/DS0 Analyzer Option.

T-BERD 310 Results Interpretation

Except for the BPV category, level, power, pulse shape, and jitter results (since the DS3 signal is internally dropped from the SONET signal), the other results (logic, parity, and frame) are applicable when testing a DS3 signal dropped from a SONET signal.

310-1 DS1 Receiver Setup and Analysis

1. **310-1 DS1 SOURCE switch**
   Select SONET DROP.

2. **310-1 RESTART switch**
   Clear the old results and start a new test.

3. **310-1 Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

4. **310-1 RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 Results Interpretation

When monitoring a DS1 payload from a SONET signal, observe the results in the LOGIC, FRAME, and SIGNAL categories.

NOTE: The BPV category and RX LVL dBdsx result are not applicable since the DS1 channel is dropped internally from within a SONET signal.

LOGIC Category

Logic error results — DS1 bit error rate testing (BERT) involves transmitting a DS1 test pattern from the DS1 input and dropping the same DS1 signal out of the SONET signal. The transmitted and received signals are compared. Any change in the bit patterns is counted as a bit error. Verification that the test pattern is received through the SONET device also insure continuity along the entire transmission path.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

SIGNAL Category

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification, the result automatically appears in the SUMMARY category.

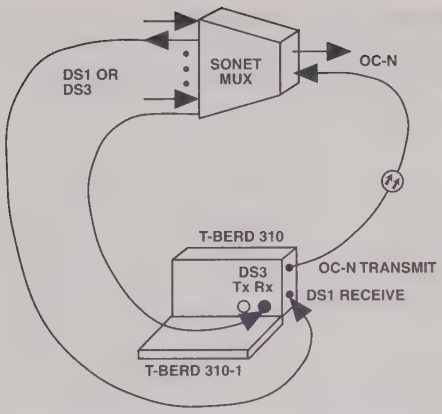
10.3 TESTING HIGH-SPEED (SONET) TO LOW-SPEED (DS3/DS1) CIRCUITS

- Test SONET multiplexer (SM), add/drop multiplexer (ADM), or digital cross-connect system (DCS) circuit functionality from the high-speed SONET STS-1 or OC-n (n is 1, 3, or 12) side to the low-speed DS1 or DS3 side while dropping and analyzing the DS3 or DS1 payload from the SONET signal.

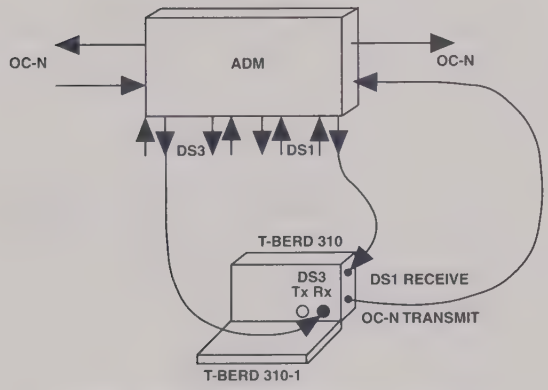
- Requires the 310-1 and either the 310-12, 310-13R and 310-13T, or 310-14R and 310-14T option.

Figure 10-3 illustrates how the T-BERD 310 connects to the SONET circuit to transmit the SONET signal with either a DS3 or DS1 payload and analyze the received DS3 or DS1 payload. The following application is divided into five parts (use the appropriate DS3 or DS1 application):

- T-BERD 310 SONET Transmitter Setup
- T-BERD 310 DS3 Transmitter Setup
- T-BERD 310 DS3 Receiver Setup and Analysis
- 310-1 DS1 Transmitter Setup
- 310-1 DS1 Receiver Setup and Analysis



TESTING SONET MULTIPLEXERS (HIGH- TO LOW-SPEED)



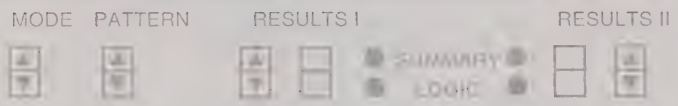
TESTING ADD/DROP MULTIPLEXERS (HIGH- TO LOW-SPEED)

T-BERD 310 SONET Transmitter Setup

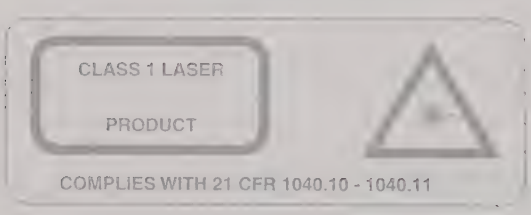
1. **AUX/MODE switches**
   Select the SONET TX auxiliary group.

2. **PATTERN/RESULTS switches**
   Select the SONET OUTPUT auxiliary function and the desired side-panel SONET output as indicated below (step does not apply to the 310-13T):

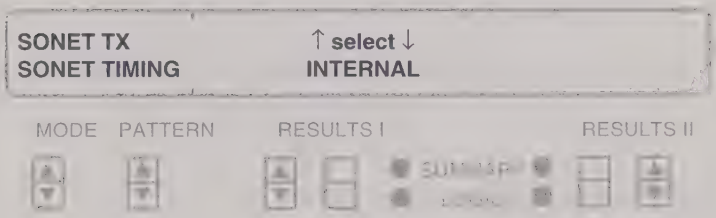
SONET TX SONET OUTPUT	↑ select ↓ OC-3	↑ select ↓ STS ID 1



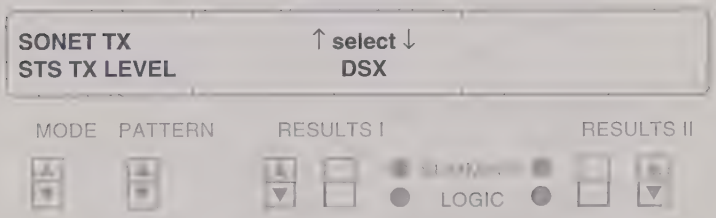
SONET OUTPUT Auxiliary Function				
Selection	**STS-1**	**OC-1**	**OC-3**	**OC-12**
STS ID	—	—	1 to 3	1 to 12
Connector	STS-1 TRANSMIT	OC-1/OC-3 TRANSMIT	OC-1/OC-3 TRANSMIT	OC-12 TRANSMIT
Option	310-14T	310-14T	310-14T	310-12



3. **PATTERN/RESULTS switch**
   Select the SONET TIMING auxiliary function and the desired transmit timing source (internal, external DS1 BITS clock, or recovered).



4. **PATTERN/RESULTS switch**
   If testing an STS-1 signal, select the STS TX LEVEL auxiliary function and set the STS-1 signal output level.



5. **AUX switch**
   Exit the auxiliary functions.

SONET transmit connections

Connect a SONET cable from one of the following output connections to the SONET circuit input connection:

- STS-1 TRANSMIT
- OC-1/OC-3 TRANSMIT
- OC-12 TRANSMIT

Clean optical connections with denatured alcohol before attaching them to the T-BERD 310.

T-BERD 310 DS3 Transmitter Setup

MODE switch

Select appropriate framing mode, e.g., to test a non-channelized DS3 signal select M13 or C-BIT, to test a channelized DS3 signal select MUXED C-BIT or MUXED M13.

PATTERN switch

Select appropriate test pattern, e.g., to test a non-channelized DS3 signal select 2^23-1, 2^20-1, etc., to test a channelized DS3 signal select T1ESF QRSS, T1D4 QRSS, etc.

TRANSMIT TIMING switch

Select INT.

AUX/MODE switches

Select the SONET TX auxiliary group.

PATTERN/RESULTS switches

For the 310-12, 310-13T, and 310-14T options, select the SONET INSERT auxiliary function and the DS3 ASYN INT payload as indicated below:

SONET TX	**↑ payload ↓**
SONET INSERT	**DS3 ASYN INT**

AUX switch

Exit the auxiliary functions.

T-BERD 310 DS3 Receiver Setup and Analysis

DS3 SOURCE switch

Select EXT.

RESTART switch

Clear the old results and start new test.

Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

4. **RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the DS3 payload, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

DS1 DROP CHANNEL switch (optional)
If the DS3 signal is properly framed for MUXED M13 or MUXED C-BIT, DS1 channels can be dropped and monitored by the 310-1 DS1/DS0 Analyzer Option.

T-BERD 310 Results Interpretation

When performing an out-of-service DS3 bit error rate test, observe the results in the LOGIC, BPV, PARITY, FRAME , and SIGNAL categories. Refer to Section 4.1 for additional information on the test results.

T-BERD 310-1 DS1 Transmitter Setup

1. **310-1 MODE switch**
   Select appropriate framing mode, e.g., T1 D4 or T1 ESF.

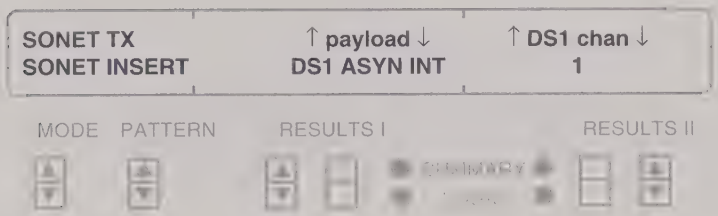
2. **310-1 PATTERN switch**
   Select appropriate DS1 test pattern, e.g., QRSS.

3. **310-1 TRANSMIT TIMING switch**
   Select INTERNAL.

310-1 CODE switch
Select either AMI or B8ZS.

5. **AUX/MODE switches**
   Select the SONET TX auxiliary group.

6. **PATTERN/RESULTS switch**
   For the 310-12, 310-13T, and 310-14T options, select the SONET INSERT auxiliary function and the desired DS1 ASYN INT, DS1 BIT INT, DS1 BYTE INT, or VT1.5 UNEQ payload and DS1 channel (1 to 28) as indicated below:



7. **AUX switch**
   Exit the auxiliary functions.

310-1 DS1 Receiver Setup and Analysis

1. **310-1 DS1 SOURCE switch**
   Select EXT INPUT.

2. **310-1 RESTART switch**
   Clear the old results and start a new test.

310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

310-1 RESULTS I test results

Select the SUMMARY category. If no errors are detected, "ALL RESULTS OK" appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

310-1 Results Interpretation

When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories. Refer to Section 4.2 for additional information on the test results.

AUXILIARY FUNCTIONS

T-BERD 310 Auxiliary Functions

310-1 DS1/DS0 Analyzer Option
Auxiliary Functions

AUXILIARY FUNCTIONS

11.1 T-BERD 310 AUXILIARY FUNCTIONS

AUX switch — Press this switch to access the auxiliary functions.

MODE switch — Press this switch to scroll through the auxiliary groups.

PATTERN switch — Press this switch to scroll through the auxiliary functions of the selected auxiliary group.

RESULTS I and RESULTS II switches — These switches are used in combination to change or enter information into the selected auxiliary function.

Group (MODE Switch)	Function (PATTERN Switch)	Description
ERR INSERT		DS3 Error Insertion Group
	LOG/BPV RT	Logic and BPV Error Insertion Rate
	FRAME ERROR	M-Frame Error Insertion Rate
	LOG/BPV BUR	Logic and BPV Error Insertion Burst Duration
ERR RECEIVE		DS3 Received Signal Error Group
	ERROR THR	Logic, BPV, and Frame Errored Second Rate Threshold
	PAT LOSS THR	Pattern Loss Threshold
	PAR ERR RT	Parity Category Error Rate Calculation
	FRM LOSS THR	Frame Synchronization Loss Threshold

Group (MODE Switch)	Function (PATTERN Switch)	Description
MUXED TX		Multiplexed Loop Code Group
	DS1 LP CODE	DS1 Loop Code Select
	PGM LPUP	Programmable Loop-Up Code
	PGM LPDN	Programmable Loop-Down Code
TIME		Time and Date Group
	SET TIME	Set Time
	SET DATE	Set Date
	TEST LENGTH	Set Test Length
PRINT		Printer/Remote Control Interface Group
	INTERVAL	Timed Printout Interval
	MODE	Printout Mode
	FORMAT	Printout Format
	CUSTOM	Customized Printout Contents
	GRAPH	Print Graph
	BAUD RATE	RS-232 Interface Baud Rate
	PARITY	RS-232 Interface Parity
	TERMINATOR	Printout Line Terminator
	WIDTH	Printout Line Width
	PORT	Printer/Remote Control Interface Port Selection (310-6 option)
MISC		Miscellaneous Group
	USER1	User-Programmable Test Pattern
	TX X-BIT	X-Bit Transmission
	BLU SIG CRI	Blue Signal Detection Criteria
	DS1 LINECODE	DS1 Drop Output Line Coding
	BEEP CRI	Beep CriteriaCoding
	PULSE MASK	Pulse Shape Mask
	FEAC ALARMS	DS3 FEAC Alarm Control
	FEAC LOOP	DS3 FEAC Message Loopback Control

Group (MODE Switch)	Function (PATTERN Switch)	Description
	LCD CONTRAST	Display Contrast Control (310-1 option)
	DS1 SIG BITS	DS1 Signaling Transfer Mode (310-13R/T pair or 310-14R/T pair option)
	DS1 BITS CLK	DS1 Building Integrated Timing Source (BITS) Clock Termination (310-13T or 310-14T option)
SONET RX		SONET RX Group (310-4 and 310-4A options)
	SONET INPUT	SONET Input Signal Source (310-4A option)
	DS1 DROP OUT	DS1 Dropout Source
	SONET DS1 CH	SONET DS1 Channel Select
	STS RX LEVEL	STS Receive Level
SONET RX		SONET RX Group (310-12, 310-13R, and 310-14R options)
	SONET INPUT	SONET Input Signal Source
	SONET DROP	SONET Dropped Payload Format
	DS1 DROP OUT	DS1 Drop Output Source
	STS RX LEVEL	STS Receive Level
	SONET DCC	SONET Data Communication Channel Insert Control
SONET TX		SONET TX Group (310-12, 310-13T and 310-14T options)
	SONET OUTPUT	SONET Output Signal Source
	SONET INSERT	SONET Insert Signal Source
	SONET TIMING	SONET Transmit Timing Source
	STS TX LEVEL	STS Transmit Level

Group (MODE Switch)	Function (PATTERN Switch)	Description
	SONET ERR RT	SONET Error Rate Select
	SONET ERR IN	SONET Error Insertion Select
	SONET ALARM	SONET Alarm Insertion Select
	SPE POINTER	Synchronous Payload Envelope Pointer Insertion Select
	PATH TRACE	Path Trace Message Insertion Control
	ORDERWIRE	Orderwire Channel Control
JITTER		DS3 Jitter Group (310-5 option)
	JIT FILTER	Jitter Bandpass Filter Select
	JIT SCALE	Jitter Amplitude Scale Select

11.2 310-1 DS1/DS0 ANALYZER OPTION AUXILIARY FUNCTIONS

AUX switch — Press this switch to access the auxiliary functions.

PATTERN switch — Press this switch to scroll through the auxiliary functions.

RESULTS I and RESULTS II switches — These switches are used in combination to change or enter information into the selected auxiliary function.

Displayed Name	Description
USER1	User 1 Programmable Test Pattern (100000)
PGM LPUP	Programmable Loop-Up Code (10000)
PGM LPDN	Programmable Loop-Down Code (100)
LP CODE	Loop Code Select (CSU)
ESF LOOP	ESF Loop Code Select (IN BAND)
PRM	ESF Datalink Performance Report Message Control (OFF/ON)
DATAPORT	DATAPORT Connector Output (DS0)
CUSTOM	Customized Printout Format (All OFF)
SLIP REF[1]	DS1 Timing Slip Reference Source (PRI DS3 DROP)

[1] Requires the 310-9A Enhanced ESF/DS1 Timing Slips Option.

T-BERD 310 TEST RESULTS

Signal Status LED Definitions

Signal Alarm LED Definitions

SUMMARY Category

LOGIC Category

BPV Category

PARITY Category

FRAME Category

SIGNAL Category

SONET Category

TIME Category

12.1 SIGNAL STATUS LED DEFINITIONS

The Status LEDs are divided into two groups labeled PRIMARY and SECONDARY. The Primary Status LEDs (except for the SONET Present LED) refer to the signal received through the PRIMARY DS3 RECEIVE INPUT jack. The Primary Status LEDs also indicate the condition of the DS3 signal dropped from a SONET DS3 payload. The Secondary Status LEDs refer to the DS3 signal received through the SECONDARY DS3 RECEIVE jack when the 310-3 DS1 Insert Option is installed. The Status LEDs are described as follows:

Signal Present — Illuminates when the T-BERD 310 detects multiple DS3 pulses. If the received signal is lost, the LED goes out and the Signal Loss LED illuminates.

Frame Sync — Illuminates when the T-BERD 310 acquires M13 or C-bit frame synchronization. If the received framing format is lost, the LED goes out and the Frame Loss LED illuminates.

C-Bit Frame — Illuminates when the T-BERD 310 acquires C-bit frame synchronization.

Idle Present — Illuminates when the T-BERD 310 detects a DS3 Idle Signal.

DS2 Frame Sync — Illuminates when the T-BERD 310 synchronizes to the DS2 framing format corresponding to the dropped DS1 channel. The T-BERD 310 must be synchronized with the DS2 framing format before a DS1 signal can be inserted. If the received DS2 framing format is lost, the LED goes out and the DS2 Frame Loss LED illuminates.

Pattern Sync — Illuminates when the T-BERD 310 synchronizes to the test pattern displayed in the PATTERN window. If pattern synchronization is lost, the LED goes out and the Pattern Loss LED illuminates.

SONET Present — Illuminates only when the T-BERD 310 detects a valid SONET signal from either the side-panel STS-1 RECEIVE jack or OC-1/3 RECEIVE connector (side panel) of a SONET drop option.

12.2 SIGNAL ALARM LED DEFINITIONS

The Alarm LEDs provide information about the current and historical alarm conditions related to the received DS3 signal. The Alarm LEDs are divided into two groups labeled PRIMARY and SECONDARY with two columns (current and history) each. The Primary Alarm LEDs (except for the SONET Loss LED) refer to the signal received through the PRIMARY DS3 RECEIVE INPUT jack. The Primary Alarm LEDs also indicate the condition of the DS3 signal dropped from a SONET DS3 payload. The Secondary Alarm LEDs refer to the signal received through the SECONDARY DS3 RECEIVE jack (side panel) when the 310-3 DS1 Insert Option is installed.

The Alarm LEDs (inside columns) illuminate when an alarm condition occurs and remain illuminated as long as the alarm exists. When the alarm condition is cleared, the Alarm LED goes out and the associated History LED (outside columns) illuminates. The History LEDs indicate past occurrences of the alarm and remain illuminated until either the **HISTORY RESET** switch is pressed or a test restart is initiated. The Primary Alarm LEDs are described as follows:

Signal Loss — Illuminates when DS3 pulses are no longer detected after initial signal detection. When the DS3 pulses are detected again, the LED goes out, and the associated History LED and the Signal Present LED illuminate.

Frame Loss — Illuminates when the T-BERD 310 loses DS3 frame synchronization. When DS3 framing is detected again, the LED goes out, and the associated History LED and the Frame Sync LED illuminate. The FRM LOSS THR auxiliary function sets the frame loss criteria.

DS2 Frame Loss — Illuminates when the T-BERD 310 loses frame synchronization to the DS2 signal for the corresponding dropped DS1 channel. When DS2 framing is detected again, the LED goes out, and the associated History LED and the DS2 Frame Sync LED illuminate.

Pattern Loss — Illuminates when the T-BERD 310 loses DS3 pattern synchronization. When the pattern is resynchronized again, the LED goes out, and the associated History LED and the Pattern Sync LED illuminate. The PAT LOSS THR auxiliary function sets the pattern loss criteria.

Blue (AIS) — Illuminates when the T-BERD 310 detects the Blue Signal (Alarm Indication Signal). When the Blue Signal is no longer detected, the LED goes out and the associated History LED illuminates. The BLU SIG CRI auxiliary function sets Blue Signal detection criteria.

Yellow — Illuminates when the T-BERD 310 detects the Yellow Alarm or Far-End Out-of-Frame (FEOOF) signal (X-bits set to zero). When the Yellow Alarm is no longer detected, the LED goes out and the associated History LED illuminates.

Far-End Alarm — Illuminates when the T-BERD 310 detects Far-End Alarm and Control (FEAC) messages in the C-bit parity framing format (third C-bit in the M1 subframe). When the Far-End Alarm is no longer detected, the LED goes out and the associated History LED illuminates. The alarm messages are reported in the SUMMARY category.

SONET Loss — Illuminates only when the T-BERD 310 no longer detects a valid SONET signal from either the side-panel STS-1 RECEIVE jack or OC-1/3 RECEIVE connector (side panel) of a SONET drop option. When a valid SONET signal is detected again, the LED goes out, and the associated History LED and the SONET Present LED illuminate.

Power Loss — Illuminates when the T-BERD 310 regains power after power was lost.

HISTORY RESET switch — This switch clears all History LEDs on the T-BERD 310. This switch does not restart a test, nor does it affect any of the Alarm LEDs or accumulated results. It is not operable when the **DISPLAY HOLD** switch is activated. The **RESTART** switch also clears the History LEDs.

12.3 SUMMARY CATEGORY

When all SUMMARY results are error-free, the message "ALL RESULTS OK" is displayed. When an error is detected, the appropriate test result appears in the SUMMARY category window (the results are identified in the following sections). If no signal is detected, "ALL RESULTS UNAVAILABLE" appears in the display. If "N/A" appears in the display, the result does not apply to the current test configuration.

In addition to the out-of specification test results, the following Far-End Alarm messages also appear in the primary and secondary SUMMARY categories as FEAC Codes.

COMM EF NSA
Common Equipment Failure, Non-Service Affecting
(Type 2 equipment failure)

DS1 EF NSA
DS1 Equipment Failure, Non-Service Affecting
(Type 2 equipment failure)

DS1 EF SA
DS1 Equipment Failure, Service Affecting
(Type 1 equipment failure)

DS3 AIS RX
DS3 Alarm Indication Signal Received

DS3 EF NSA
DS3 Equipment Failure, Non-Service Affecting
(Type 2 equipment failure)

DS3 EF SA
DS3 Equipment Failure, Service Affecting
(Type 1 equipment failure)

DS3 IDLE RX
DS3 Idle Signal Received

DS3 L/H
DS3 Loss-of-Signal/High Bit Error Ratio

DS3 OOF
DS3 Out-of-Frame, Loss of DS3 Frame Synchronization

MULT DS1 L/H
Multiple DS1 Loss-of-Signal/High Bit Error Ratio

SING DS1 L/H
Single DS1 Loss-of-Signal/High Bit Error Ratio

12.4 LOGIC CATEGORY

BIT ERRORS
Bit Errors — The number of received pattern bits which have a value opposite that of the corresponding transmitted bit pattern since initial DS3 pattern synchronization. The result also appears in the SUMMARY category (count > 0). The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

BIT ERR RT
Bit Error Rate — The ratio of pattern bit errors to received pattern bits over the previous block of 10^8 bits.

AV BIT ERT
Average Bit Error Rate — The ratio of pattern bit errors to the total number of received pattern bits while DS3 pattern synchronization is present.

BIT ERR SEC

Bit Errored Seconds — The number of seconds during which one or more pattern bit errors occurred since initial DS3 pattern synchronization.

BIT %EFS

Bit, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no pattern bit errors were detected, to the total number of seconds while DS3 pattern synchronization is present.

BIT THR ES

Bit, Threshold Errored Seconds — The number of seconds during which the pattern bit error rate exceeded or equaled the user-defined threshold. The threshold is set through the ERROR THR auxiliary function. The BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

SYNC ES

Synchronous Errored Seconds — The number of seconds during which at least one pattern bit error has occurred. Each second is initiated by, and synchronized to, a pattern bit error.

SYNC L SEC

Synchronization Loss Seconds — The number of seconds during which the receiver has lost pattern synchronization, even momentarily, since initial DS3 pattern synchronization.

SLIPS

Slips — The number of times the received pattern becomes skewed relative to the expected (i.e., internally generated) test pattern. When a slip is detected, the T-BERD 310 automatically resynchronizes to the received pattern. However, pattern bit errors are not suppressed during this process. Pattern slips are available only when using pseudorandom patterns. The result also appears in the SUMMARY category (count > 0).

The following G.821 test results require the 310-10 G.821 Results Option.

AVAIL SEC

Available Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is less than 10^{-3}.

%AVAIL SEC

% Available Seconds — The ratio, expressed as a percentage, of available seconds to the total elapsed seconds since pattern synchronization.

SEV ERR SEC

Severely Errored Seconds — A count of seconds during which the bit error rate is worse than 10^{-3} within the available time.

%SEVERR SEC

% Severely Errored Seconds — The ratio, expressed as a percentage, of severely errored seconds to the number of available seconds.

CSES

Consecutive Severely Errored Seconds — A count of three or more contiguous severely errored seconds in which a bit error rate worse than 10^{-3} in each second.

DEG MIN

Degraded Minutes — A count of minutes during which the bit error ratio is worse than 10^{-6} and less than 10^{-3}.

%DEG MIN

% Degraded Minutes — The ratio, expressed as a percentage, of degraded minutes to the number of available non-severely errored minutes.

UNAVAIL SEC

Unavailable Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is greater than or equal to 10^{-3}.

BIT ERR SEC

Bit Errored Seconds — The number of seconds during which one or more pattern bit errors occurred since initial DS3 pattern synchronization.

BIT %EFS

Bit, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no pattern bit errors were detected, to the total number of seconds while DS3 pattern synchronization is present.

BIT THR ES

Bit, Threshold Errored Seconds — The number of seconds during which the pattern bit error rate exceeded or equaled the user-defined threshold. The threshold is set through the ERROR THR auxiliary function. The BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

SYNC ES

Synchronous Errored Seconds — The number of seconds during which at least one pattern bit error has occurred. Each second is initiated by, and synchronized to, a pattern bit error.

SYNC L SEC

Synchronization Loss Seconds — The number of seconds during which the receiver has lost pattern synchronization, even momentarily, since initial DS3 pattern synchronization.

SLIPS

Slips — The number of times the received pattern becomes skewed relative to the expected (i.e., internally generated) test pattern. When a slip is detected, the T-BERD 310 automatically resynchronizes to the received pattern. However, pattern bit errors are not suppressed during this process. Pattern slips are available only when using pseudorandom patterns. The result also appears in the SUMMARY category (count > 0).

The following G.821 test results require the 310-10 G.821 Results Option.

AVAIL SEC

Available Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is less than 10^{-3}.

%AVAIL SEC

% Available Seconds — The ratio, expressed as a percentage, of available seconds to the total elapsed seconds since pattern synchronization.

SEV ERR SEC

Severely Errored Seconds — A count of seconds during which the bit error rate is worse than 10^{-3} within the available time.

%SEVERR SEC

% Severely Errored Seconds — The ratio, expressed as a percentage, of severely errored seconds to the number of available seconds.

CSES

Consecutive Severely Errored Seconds — A count of three or more contiguous severely errored seconds in which a bit error rate worse than 10^{-3} in each second.

DEG MIN

Degraded Minutes — A count of minutes during which the bit error ratio is worse than 10^{-6} and less than 10^{-3}.

%DEG MIN

% Degraded Minutes — The ratio, expressed as a percentage, of degraded minutes to the number of available non-severely errored minutes.

UNAVAIL SEC

Unavailable Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is greater than or equal to 10^{-3}.

12.5 BPV CATEGORY

VIOLATIONS

Bipolar Violations — The number of bipolar violations (BPVs) detected since the beginning of the test. Intentional B3ZS code violations are excluded from the count. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

BPV ERR RT

BPV Error Rate — The ratio of BPVs to received bits over the previous block of 10^8 bits.

AV BPV ERT

Average BPV Error Rate — The ratio of BPVs to the total number of received bits since the beginning of the test.

BPV ERR SEC

BPV Errored Seconds — The number of seconds during which one or more BPVs occurred since the beginning of the test.

BPV %EFS

BPV, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no BPVs were detected, to the total number of seconds since the beginning of the test.

BPV THR ES

BPV Threshold Errored Seconds — The number of seconds during which the BPV rate exceeded or equaled the user-defined threshold. The threshold is set through the ERROR THR auxiliary function. The BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

12.6 PARITY CATEGORY

PAR ERRORS

Parity (P-bit) Errors — The number of parity errors detected since initial DS3 frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

PAR ERR RT

Parity (P-bit) Error Rate — The ratio of parity errors to (1) the number of bits over which parity was calculated (Bit mode), or (2) the number of DS3 M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of PAR ERR RT auxiliary function.

AV PAR ERT

Average Parity (P-bit) Error Rate — The ratio of parity errors to (1) the number of bits over which parity was calculated (Bit mode), or (2) the number of DS3 M-frames received (Block mode). The error rate is computed while DS3 frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the PAR ERR RT auxiliary function.

PAR ERR SEC

Parity (P-bit) Errored Seconds — The number of seconds during which one or more parity errors occurred since initial DS3 frame synchronization.

PAR %EFS

Parity (P-bit), Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no parity errors were detected, to the total number of seconds while DS3 frame synchronization is present.

C-BIT ERRORS

C-bit Parity Errors — The number of parity errors detected since initial DS3 C-bit frame synchronization. The result also appears in the SUMMARY category (count > 0) and the

Secondary DS3 category results. The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

C-BIT ERR RT

C-bit Parity Error Rate — The ratio of C-bit parity errors to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of the PAR ERR RT auxiliary function.

AV C-BIT ERT

Average C-bit Parity Error Rate — The ratio of C-bit parity errors to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed while DS3 C-bit frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the PAR ERR RT auxiliary function.

C-BIT TYPE A

C-bit Parity Errored Seconds, Type A — The number of seconds during which one and only one C-bit parity error occurred since initial DS3 C-bit frame synchronization.

C-BIT TYPE B

C-bit Parity Errored Seconds, Type B — The number of seconds during which 2 to 44 C-bit parity errors occurred since initial DS3 C-bit frame synchronization.

C-BIT TYPE C

C-bit Parity Errored Seconds, Type C — The number of seconds during which more than 44 C-bit parity errors occurred since initial DS3 C-bit frame synchronization.

C-BIT %EFS

C-bit Parity, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no C-bit parity errors were detected, to the total number of seconds while DS3 C-bit frame synchronization is present.

FEBE

Far-End Block Errors — The number of far-end block errors (FEBEs) detected since initial DS3 C-bit frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

FEBE RT

Far-End Block Error Rate — The ratio of FEBEs to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of the PAR ERR RT auxiliary function.

AV FEBE RT

Average Far-End Block Error Rate — The ratio of FEBEs to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed while DS3 C-bit frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the PAR ERR RT auxiliary function.

FEBE TYPE A

Far-End Block Errored Seconds, Type A — The number of seconds during which one and only one FEBE occurred since initial DS3 C-bit frame synchronization.

FEBE TYPE B

Far-End Block Errored Seconds, Type B — The number of seconds during which 2 to 44 FEBEs occurred since initial DS3 C-bit frame synchronization.

FEBE TYPE C

Far-End Errored Seconds, Type C — The number of seconds during which more than 44 FEBEs occurred since initial DS3 C-bit frame synchronization.

FEBE %EFS

Far-End Block Error, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no FEBEs were detected, to the total number of seconds while DS3 C-bit frame synchronization is present.

12.7 FRAME CATEGORY

FRM ERRORS

Frame Errors — The number of frame errors detected since initial DS3 frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

FRM ERR RT

Frame Error Rate — The ratio of frame errors to received framing bits over the previous block of 10^8 bits.

AV FRM ERT

Average Frame Error Rate — The ratio of frame errors to the total number of received framing bits while DS3 frame synchronization is present.

FRM ERR SEC

Frame Errored Seconds — The number of seconds during which one or more frame errors occurred since initial DS3 frame synchronization.

FRM %EFS

Frame, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no frame errors were detected, to the total number of seconds while DS3 frame synchronization is present.

FRM THR ES

Frame Threshold Errored Seconds — The number of seconds during which the frame error rate exceeded or equaled the

user-defined threshold. The threshold is set through the ERROR THR auxiliary function. The BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

FRM LOSS CNT

DS3 Frame Loss Count — The number of DS3 frame losses occurring after initial frame synchronization.

FEOOF SEC

Far-End Out-of-Frame Seconds — The number of seconds during which the received X-bits are zero within the one second interval.

NEOOF SEC

Near-End Out-of-Frame Seconds — The number of seconds during which an out-of-frame condition or an AIS (Alarm Indication Signal) is detected.

DS2 FRM ERR

DS2 Frame Errors — The number of DS2 frame errors detected since initial DS2 frame synchronization. The result applies only to the DS2 signal which contains the DS1 (or E1) channel being dropped. The count is reset when the selected dropped channel is changed such that the new channel being dropped corresponds to a different DS2 signal. The result also appears in the SUMMARY category (count > 0). The BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

DS2 FRM ERT

DS2 Frame Error Rate — The ratio of detected DS2 frame errors to the total DS2 framing bits received. The result applies only to the DS2 signal that contains the DS1 channel being dropped. The count is reset when the selected dropped DS1 channel is changed such that the new channel being dropped corresponds to a different DS2 signal.

DS2 AV F ERT

DS2 Average Frame Error Rate — The ratio of DS2 frame errors to the total number of received framing bits while DS2 frame synchronization is present.

TX X-BIT

Transmitted X-bit — The current setting of the transmitted X-bits when in a framed mode. The transmitted X-bits are set through the TX X-BIT auxiliary function.

RX X-BIT

Received X-bit — The current status of the received X-bits when in a framed mode. The result is available after receiving DS3 frame synchronization.

12.8 SIGNAL CATEGORY

SIG L SEC

Signal Loss Seconds — The number of seconds during which the received DS3 signal was lost for all or part of a second since initial signal detection.

TX FREQ

Transmit Frequency — The frequency of the transmit clock measured in Hz.

RX FREQ

Receive Frequency — The frequency of the clock recovered from the received data measured in Hz. The result also appears in the SUMMARY category (frequency >/< 1000 Hz) and the Secondary DS3 category results.

POWER

Receive Signal Power — The power level of the received DS3 signal measured in dBm.

LEVEL

Receive Signal Level — The level of the received DS3 signal in volts peak.

PULSE SHAPE

Pulse Shape — A PASS/FAIL result which shows whether the DS3 pulse shape is within the boundary of the specified pulse mask. The pulse shape mask is set through the PULSE MASK auxiliary function.

PULSE WIDTH

Pulse Width — The pulse width of the DS3 pulse measured in nanoseconds.

RISE TIME

Pulse Rise Time — The time interval between the 10% and 90% points of the rising edge of the DS3 pulse measured in nanoseconds.

FALL TIME

Pulse Fall Time — The time interval between the 10% and 90% points of the falling edge of the DS3 pulse measured in nanoseconds.

WB JITTER

Wideband Jitter — The current wideband (10 Hz to 400 kHz) jitter amplitude, expressed in peak-to-peak UIs. The result only appears in the jitter AUTO and ANSI WIDEBAND mode. The result is controlled by the DS3 JITTER auxiliary group.

MAX WB JIT

Maximum Wideband Jitter — The maximum peak-to-peak wideband jitter amplitude, expressed in peak-to-peak UIs, since initial signal presence or test restart. The result only appears in the jitter AUTO and ANSI WIDEBAND mode. The result is controlled by the DS3 JITTER auxiliary group.

HB JITTER

Highband Jitter — The current highband (30 kHz to 400 kHz) jitter amplitude, expressed in peak-to-peak UIs. The result only appears in the jitter AUTO and ANSI HIGHBAND mode. The result is controlled by the DS3 JITTER auxiliary group.

MAX HB JIT

Maximum Highband Jitter — The maximum peak-to-peak highband jitter amplitude, expressed in peak-to-peak UIs, since

initial signal presence or test restart. The result only appears in the jitter AUTO and ANSI HIGHBAND mode. The result is controlled by the DS3 JITTER auxiliary group.

12.9 SONET CATEGORY

Section Overhead Test Results

FRM WORD ERR

Frame Word Errors — Counts the number of errored frame alignment signal (FAS) subsets (subset of bytes A1 and A2) received since gaining initial frame synchronization.

SON SEF SEC

SONET Severely Errored Frame Seconds — Counts the number of seconds in which one or more loss of frame (LOF) alarms have occurred since gaining initial frame synchronization. A severely errored frame (SEF) is defined as four consecutive STS-N frames received with errored frame words. An LOF is defined as SEFs persisting for 3 ms or a random unframed signal for 625 microseconds.

SON LOS SEC

SONET Loss of Signal Seconds — Counts the number of seconds in which one or more SONET loss of signal (LOS) events occur. An LOS is defined as an all zeros pattern which lasts for least 100 microseconds. An LOS is removed after two consecutive valid frame alignment signals are detected without intervening loss of signal.

SON RX FREQ

SONET Receive Frequency — Displays the recovered clock frequency of the received SONET signal in hertz.

SON TX FREQ

SONET Transmit Frequency — Displays the frequency of the transmitted SONET signal in hertz.

SECT BIP ERR

Section BIP Errors — Counts the number of times the Section BIP byte (B1) indicates an error in the previous frame since initial SONET frame synchronization. Up to eight section BIP errors can be counted in a single frame.

SECT EQU BER

Section Equivalent Bit Error Rate — Presents an equivalent Section bit error rate (BER) which is derived from the received section BIP error count since initial SONET frame synchronization.

SECT BIP ES

Section BIP Errored Seconds — Counts the number of seconds in which one or more Section BIP errors occurred since initial SONET frame synchronization. The errored second interval is not synchronous to the occurrence of the BIP error.

SECT BIP ESA

Section BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Section BIP error occurred, and no LOF or LOS alarms occurred.

SECT BIP ESB

Section BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than x Section BIP errors occurred, and no LOF or LOS alarms occurred. x is defined in Table 12-1 for each rate.

SECT BIP ESA

Section BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Section BIP error occurred, and no LOF or LOS alarms occurred.

SECT BIP ESB

Section BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than x Section BIP errors occurred, and no LOF or LOS alarms occurred. x is defined in Table 12-1 for each rate.

Table 12-1
Errored Second BIP Thresholds

Rate	BIP Errors (x)	Equivalent BER
Section		
STS-1/OC-1	2500	4.8E-5
OC-3	2500	1.6E-5
OC-12	8800	1.4E-5
Line		
STS-1/OC-1	2500	4.9E-5
OC-3	2500	1.6E-5
OC-12	10,000	1.6E-5
Path		
STS-1/OC-1	2400	4.7E-5
VT		
VT1.5	600	3.6E-4

SECT BIP SES

Section BIP Severely Errored Seconds — Counts the number of seconds in which x or more Section BIP errors occurred since initial SONET frame synchronization. x is defined in Table 12-1 for each rate.

Line Overhead Test Results

LINE BIP ERR

Line BIP Errors — Counts the number of times in which the Line BIP byte (B2) indicates an error in the previous frame since initial SONET frame synchronization. Up to eight Line BIP errors can be counted in a single frame.

LINE EQU BER

Line Equivalent Bit Error Rate — Presents an equivalent Line BER which is derived from the received Line BIP error count since initial SONET frame synchronization.

LINE BIP ES

Line BIP Errored Seconds — Counts the number of seconds in which one or more Line BIP errors occurred since initial SONET frame synchronization. The errored second interval is not synchronous to the occurrence of the BIP error.

LINE BIP ESA

Line BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Line BIP error occurred, and no LOF or LOS alarms occurred.

LINE BIP ESB

Line BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than x Line BIP errors occurred, and no LOF or LOS alarms occurred. x is defined in Table 12-1 for each rate.

LINE BIP SES

Line BIP Severely Errored Seconds — Counts the number of seconds in which x or more Line BIP errors occurred since initial SONET frame synchronization. x is defined in Table 12-1 for each rate.

LINE UAS

Line Unavailable Seconds — Counts the number of seconds in which the line is not available based on counts of consecutive line severely errored seconds.

LINE AIS SEC

Line AIS Seconds — Counts the number of seconds in which one or more line AIS alarms occurred.

LINE FEBE

Line FEBE — Counts the line FEBEs detected. Line far-end block errors are defined in the Z2 byte for STS-1, OC-3, and OC-12.

LINE FEBE RT

Line FEBE Rate — Presents an equivalent BER based on received line FEBE counts.

POINTER JUST

Pointer Justifications — Counts the number of times the synchronous payload envelope (SPE) pointer changed since initial SONET frame synchronization.

POINTER INC

Pointer Increments — Counts the number of times the pointer bytes (H1 and H2) indicated an increment to the path payload pointer since initial SONET frame synchronization.

POINTER DEC

Pointer Decrements — Counts the number of times the pointer bytes (H1 and H2) indicated an decrement to the path payload pointer since initial SONET frame synchronization.

POINTER NDF

Pointer New Data Flags — Counts the number of times the pointer bytes (H1 and H2) indicated an active new data flag (arbitrary change in pointer) since initial SONET frame synchronization. An active NDF occurs during a change in payload content, or after an AIS or some other failure condition. If a change in the pointer is detected for three consecutive frames, the change is counted as an NDF, even if the pointer never has an active NDF.

POINTER DATA

Pointer Data — Presents the current STS path pointer value from 0 to 782. "UNAVAILABLE" appears under a number of error conditions, such as line AIS, etc. "CONCAT" appears when receiving a concatenated payload (i.e., an STS-3c signal), and the current STS ID is set to a value other than STS ID 1. "OUT OF RANGE" appears if the pointer value is outside 0 to 782.

APS MSG CNT

APS Message Count — Counts the number of transitions occurring in the switch priority field of the line overhead byte (K1), Bits 1 to 4. This is an indication of protection switch activity; it is not a direct count of protection switches.

APS INFO

APS Information — Presents the current protection switch request message and channel as indicated by the line overhead byte (K1). The displayed messages are listed in Table 12-2. *##* is the channel number from 0 to 15. Since the APS data bytes (K1 and K2) may change rapidly during a protection switch operation, the display may not indicate every transition.

Message	Switch Request
## LOCKOUT	Lockout of Protection
## FORCE SW	Forced Switch
## SIG FAILH	Signal Fail High-priority
## SIG FAILL	Signal Fail Low-priority
## SIG DEGRH	Signal Degrade High-priority
## SIG DEGRL	Signal Degrade Low-priority
## MANUAL SW	Manual Switch
## WTR	Wait to Restore
## EXERCISE	Exerciser
## REVERSE	Reverse Request
## NO REVERT	Do Not Revert
## NO REQ	No Request

APS CONFIG

APS Configuration — Presents the current APS configuration: 1:n verses 1+1, and bidirectional verses unidirectional. This information is obtained from the APS line overhead byte (K2). Table 12-3 lists the possible APS configuration messages. The Mode appears on the left half of the result window, and Switching appears on the right half.

Table 12-3
SONET APS Configuration Result Message

Message	Switch Request
1:n	Provisioned for 1:n mode
1+1	Provisioned for 1+1 mode
Switching	
BIDIR	Provisioned for Bidirectional Switching
UNIDIR	Provisioned for Unidirectional Switching
AIS	Line AIS
RDI	Line RDI

Path Overhead Test Results

PATH BIP ERR

Path BIP Errors — Counts the number of times in which the Path BIP byte (B3) indicates an error in the previous frame since initial SONET frame synchronization. Up to eight Path BIP errors can be counted in a single frame.

PATH EQU BER

Path Equivalent Bit Error Rate — Presents an equivalent Path BER which is derived from the received Path BIP error count since initial SONET frame synchronization.

PATH BIP ES

Path BIP Errored Seconds — Counts the number of seconds in which one or more Path BIP errors occurred since initial SONET frame synchronization. The errored second interval is not synchronous to the occurrence of the BIP error.

PATH BIP ESA

Path BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Path BIP error occurred, and no LOF or LOS alarms occurred.

PATH BIP ESB

Path BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than x Path BIP errors occurred, and no LOF or LOS alarms occurred. x is defined in Table 12-1 for each rate.

PATH BIP SES

Path BIP Severely Errored Seconds — Counts the number of seconds in which x or more Path BIP errors occurred since initial SONET frame synchronization. x is defined in Table 12-1 for each rate.

PATH UAS

Path Unavailable Seconds — Counts the number of seconds in which the line is unavailable. The path is unavailable when 10 consecutive frame word errors are received, or when a condition leading to a failure (i.e., loss of signal) occurs. If the failure was preceded by one or more consecutive frame word errors, then path unavailability starts with the frame word errors. The path becomes available again after a minimum of 10 consecutive seconds without any frame word errors, or when the failure is removed, whichever is greater. All path related results count when the path is available. When the path is unavailable, only this result counts.

PATH AIS SEC

Path AIS/LOP Seconds — Counts the number of seconds in which one or more Path AIS or LOP occurs.

PATH FEBE

Path FEBE — Counts the number of Path BIP errors detected by the downstream PTE. It is calculated by summing the FEBE counter of the path status byte (G1, Bits 1 to 4) from each received frame.

PATH FEBE RT

Path FEBE Rate — Presents an equivalent BER based on received Path FEBE counts.

PATH TRACE

Path Trace Message — Displays the 64-byte path trace ASCII CLLI message which is carried in the path overhead byte (J1). The message scrolls across the results window in a ticker tape fashion, 12 characters at a time.

SIGNAL LABEL

Signal Label — Presents the payload type being carried in the current position of the current STS. The information is derived from the Path signal label (C2) and VT overhead (V5) bytes. Any C2/V5 combinations which cannot be decoded appear as "UNRECOGNIZED". Table 12-4 lists the signal label messages. The V5 byte for VT1.5 payloads is fully decoded. For other virtual tributary sizes (VT2, VT3, and VT6), only the floating/locked indication and size are shown.

Displayed Name	Description
DS4NA	DS4 North American (139.264 Mb/s)
ATM	Asynchronous Transfer Mode
DQDB	Distributed Queue Dual Bus (MAN)
DS1 ASYN	DS1 Asynchronous
DS1 ASYN L	DS1 Asynchronous, Locked Mode
DS1 BIT	DS1 Bit Synchronous
DS1 BIT L	DS1 Bit Synchronous, Locked Mode
DS1 BYTE	DS1 Byte Synchronous
DS1 BYTE L	DS1 Byte Synchronous, Locked Mode
DS3 ASYN	Asynchronous DS3
FDDI	Fiber Distributed Data Interface
PATH EQNS	Path Equipped Nonspecific
PATH UNEQ	Path Unequipped
SYNTRAN	Byte Observable SYNTRAN
UNKNOWN_xxx	Undecodable. xxx is the numeric value of the C2 byte.
VT1.5 EQNS L	VT1.5 Equipped Nonspecific, Locked Mode
VT1.5 EQNS	VT1.5 Equipped Nonspecific
VT1.5 UNAS L	VT1.5 Unassigned, Locked Mode
VT1.5 UNAS	VT1.5 Unassigned
VT1.5 UNEQ L	VT1.5 Unequipped, Locked Mode
VT1.5 UNEQ	VT1.5 Unequipped
VT2 L	VT2, Locked Mode
VT2	VT2
VT3 L	VT3, Locked Mode
VT3	VT3
VT6 L	VT6, Locked Mode
VT6	VT6

Virtual Tributary Overhead Test Results

VT BIP ERR

VT BIP Errors — Counts the number of times in which the VT BIP byte (V5, Bits 1 and 2) indicates an error in the received signal. A maximum of two VT BIP errors can be counted in each SONET frame.

VT EQU BER

VT Equivalent Bit Error Rate — Presents an equivalent VT BER which is derived from the received VT BIP error count since initial SONET frame synchronization.

VT BIP ES

VT BIP Errored Seconds — Counts the number of seconds in which one or more VT BIP errors, an AIS, or VT LOP occurred.

VT BIP ESA

VT BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one VT BIP error occurred, and no LOF or LOS alarms occurred.

VT BIP ESB

VT BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than x VT BIP errors occurred, and no LOF or LOS alarms occurred. x is defined in Table 12-1 for each rate.

VT BIP SES

VT BIP Severely Errored Seconds — Counts the number of seconds in which x or more VT BIP errors, x AIS, or VT LOP occurred. x is defined in Table 12-1 for each rate.

VT UAS

VT Unavailable Seconds — Counts the number of seconds in which the VT path is unavailable. The path is unavailable when 10 consecutive severely errored seconds are received, or when a condition leading to a failure (i.e., loss of signal) occurs. If the failure was preceded by one or more consecutive severely

errored seconds, then VT path unavailability starts with the severely errored seconds. The VT path becomes available again after a minimum of 10 consecutive seconds without any severely errored seconds, or when the failure is removed, whichever is greater. All VT path related results count when the VT path is available. When the VT path is unavailable, only this result counts.

VT AIS SEC

VT AIS/LOP Seconds — Counts the number of seconds in which one or more VT AIS or LOP occurs.

VT FEBE

VT FEBE — Counts the number of VT BIP errors detected by the downstream PTE. It is calculated by summing the FEBE counter of the path status byte (V5, Bit 3) from each received VT superframe.

VT PTR JUST

VT Pointer Justifications — Counts the number of times the VT path pointer byte (V1 and V2) changed since initial SONET frame synchronization.

VT PTR INC

VT Pointer Increments — Counts the number of times the VT pointer bytes (V1 and V2) indicated an increment to the VT payload pointer since initial SONET frame synchronization.

VT PTR DEC

VT Pointer Decrements — Counts the number of times the VT pointer bytes (V1 and V2) indicated a decrement to the VT payload pointer since initial SONET frame synchronization.

VT PTR NDF

VT Pointer New Data Flags — Counts the number of times the VT pointer bytes (V1 and V2) indicated an active new data flag (arbitrary change in pointer) since initial SONET frame synchronization. An active NDF occurs during a change in payload content, or after an AIS or some other failure condition.

VT PTR DATA

VT Pointer Data — Presents the current VT pointer value from 0 to 103. "UNAVAILABLE" appears under a number of error conditions, such as line AIS, etc. "OUT OF RANGE" appears if the pointer value is outside 0 to 103.

12.10 TIME CATEGORY

TIME

Current Time of Day — The current time of day in hours, minutes, and seconds. The time is set through the SET TIME auxiliary function.

DATE

Current Date — The current day and month. The date is set through the SET DATE auxiliary function.

ELAPSED TIME

Elapsed Time — The elapsed time in hours, minutes, and seconds since the last test restart.

TEST LENGTH

Timed Test Length — The currently set test length for a timed test in hours and minutes. The test length is set through the TEST LENGTH auxiliary function.

TIME LEFT

Timed Test Time Left — The time remaining for a timed test in hours, minutes, and seconds.

310-1 DS1/DS0 ANALYZER TEST RESULTS

Signal Status LED Definitions

Signal Alarm LED Definitions

SUMMARY Category

LOGIC Category

BPV Category

FRAME Category

SIGNAL Category

TIME Category

310-1 DS1/DS0 ANALYZER TEST RESULTS

13.1 SIGNAL STATUS LED DEFINITIONS

The following green Status LEDs provide information about the condition of the received DS1 signal. The Status LEDs are described as follows:

T1 Pulses — Illuminates when the 310-1 detects multiple T1 pulses from one of three DS1 sources: the side-panel DS1 RECEIVE jack, channelized DS3, or SONET DS1 payload. If the received signal is lost, the LED goes out and the Signal Loss LED illuminates.

Frame Sync — Illuminates when the 310-1 acquires frame synchronization. If the received framing format is lost, the LED goes out and the Frame Loss LED illuminates.

Pattern Sync — Illuminates when the 310-1 synchronizes to the test pattern displayed in the PATTERN window. If pattern synchronization is lost, the LED goes out and the Pattern Loss LED illuminates.

B8ZS — Illuminates when B8ZS clear channel coding is detected in the received DS1 signal. When B8ZS encoding is detected and the **CODE** switch is set to AMI, the message "B8ZS DETECTED" is also displayed in the SUMMARY category. The LED is only active when the **DS1 SOURCE** switch is set to EXT. INPUT (side-panel DS1 RECEIVE jack).

13.2 SIGNAL ALARM LED DEFINITIONS

The red Alarm LEDs provide information about the current and historical alarm conditions related to the received signal. These LEDs are divided into two columns (current and history). The right column illuminates when an alarm condition occurs and remains illuminated as long as the alarm exists. When the current alarm condition is cleared

(e.g., pattern sync reestablished), the associated History LED illuminates. The History LEDs indicate past occurrences of the alarm and remain illuminated until either the **HISTORY RESET** switch is pressed or a 310-1 test restart occurs. The Alarm LEDs are described as follows:

Signal Loss — Illuminates when no pulses are detected. When T1 pulses are detected again, the Alarm LED goes out, and the associated History LED and the T1 Pulses LED illuminate.

Frame Loss — Illuminates when frame synchronization is lost. When DS1 framing is detected again, the Alarm LED goes out, and the associated History LED and the Frame Sync LED illuminate.

Pattern Loss — Illuminates when pattern synchronization is lost. When the pattern is resynchronized, the Alarm LED goes out, and the associated History LED and Pattern Sync LED illuminate.

Excess Zeros — Illuminates when excess zeros are detected in AMI or B8ZS coding. When excess zeros are no longer detected, the LED goes out and the associated History LED illuminates. The LED is only active when the **DS1 SOURCE** switch is set to EXT. INPUT.

Yellow Alarm — Illuminates when a Yellow Alarm is detected. When the Yellow Alarm is no longer detected, the LED goes out and the associated History LED illuminates.

All Ones — Illuminates when all ones are detected in framed and unframed DS1 signals. When All Ones are no longer detected, the LED goes out and the associated History LED illuminates.

HISTORY RESET switch — This switch clears all History LEDs on the 310-1. This switch does not restart a test, nor does it affect any of the Alarm LEDs or accumulated results. It is not operable when the **DISPLAY HOLD** switch is activated. The **RESTART** switch also clears the History LEDs.

13.3 SUMMARY CATEGORY

When all SUMMARY results are error-free, the message "ALL RESULTS OK" is displayed. When an error is detected, the appropriate test result appears in the SUMMARY category window (the results are identified in the following sections). If no signal is detected, "ALL RESULTS UNAVAILABLE" appears in the display. If "N/A" appears in the display, the result does not apply to the current test configuration.

13.4 LOGIC CATEGORY

BIT ERRORS

Bit Errors — The number of received pattern bits which have a value opposite that of the corresponding transmitted bit pattern since initial DS1 pattern synchronization. The result also appears in the SUMMARY category (count > 0).

BIT ERR RT

Bit Error Rate — The ratio of pattern bit errors to received pattern bits since initially acquiring pattern synchronization.

ASYNC ERR SEC

Asynchronous Errored Seconds — The number of seconds during which one or more pattern bit errors occurred since initial DS1 pattern synchronization.

SYNC ERR SEC

Synchronous Errored Seconds — The number of seconds during which at least one pattern bit error has occurred. Each second is initiated by, and synchronized to, a pattern bit error.

%EFS

Bit, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no pattern bit errors were detected to the total number of seconds while DS1 pattern synchronization is present.

SYNC L SEC

Out-of-Synchronization Seconds — The number of seconds during which the receiver has lost pattern synchronization, even momentarily, since initial DS1 pattern synchronization.

SEV ERR SEC

Severely Errored Seconds — The number of seconds during which the pattern bit error rate exceeded or equaled 10^{-3} b/s.

CSES

Consecutive Severely Errored Seconds —The number of groups of three or more severely errored seconds.

SLIPS

Slips — The number of times the received pattern becomes skewed relative to the expected (i.e., internally generated) test pattern. When a slip is detected, the 310-1 automatically resynchronizes to the received pattern. However, pattern bit errors are not suppressed during this process. Pattern slips are available only when using pseudorandom patterns. The result also appears in the SUMMARY category (count > 0).

The following G.821 test results require the 310-10 G.821 Results Option.

AVAIL SEC

Available Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is less than 10^{-3}.

%AVAIL SEC

% Available Seconds — The ratio, expressed as a percentage, of available seconds to the total elapsed seconds since pattern synchronization.

%SEV ER SEC

% Severely Errored Seconds — The ratio, expressed as a percentage, of severely errored seconds to the number of available seconds.

DEG MIN

Degraded Minutes — A count of minutes during which the bit error ratio is worse than 10^{-6} and less than 10^{-3}.

%DEG MIN

% Degraded Minutes — The ratio, expressed as a percentage, of degraded minutes to the number of available minutes.

UNAVAIL SEC

Unavailable Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is greater than or equal to 10^{-3}.

13.5 BPV CATEGORY

VIOLATIONS

Bipolar Violations — The number of bipolar violations (BPVs) detected since the beginning of the test. Intentional B8ZS code violations are excluded from the count. The result also appears in the SUMMARY category (count > 0).

BPV ERR RT

BPV Error Rate — The ratio of BPVs to received bits since initially acquiring signal presence.

BPV ERR SEC

BPV Errored Seconds — The number of seconds during which one or more BPVs occurred since the beginning of the test.

FAR BPV SEC

Far-End BPV Seconds — The number of seconds during which one or more BPVs occurred in the far-end received signal. This result reports on the PRM Line-Code Violation Event Bit (LV = 1) status. Requires the 310-9A Enhanced ESF/DS1 Timing Slips Option.

13.6 FRAME CATEGORY

FRM ERRORS

Frame Errors — The number of frame errors detected since initial DS1 frame synchronization.

FRM ERR RT

Frame Error Rate —The ratio of frame errors to received framing bits since initially acquiring frame synchronization.

FRM ERR SEC

Frame Errored Seconds —The number of seconds during which one or more frame errors occurred since initial DS1 frame synchronization.

FRM SES

Frame Severely Errored Seconds — The number of seconds during which the total number of frame errors equals 12 or more (D4 framing only).

FRM L SEC

Frame Loss Seconds — The number of seconds during which one or more frame synchronization losses occurred or during which frame synchronization could not be achieved, since initial DS1 frame synchronization.

CRC ERRORS

Cyclic Redundancy Check Errors — The number of CRC errors detected since initial DS1 frame synchronization. CRC errors are counted only when ESF or ESFz framing is present in the received T1 data.

CRC ERR SEC

Cyclic Redundancy Check Errored Seconds — The number of seconds during which one or more CRC errors occurred.

CRC ERR RT

Cyclic Redundancy Check Error Rate — The ratio of CRC errors to the number of superframes received.

CRC SES

Cyclic Redundancy Check Severely Errored Seconds — The number of seconds during which the total number of CRC errors and frame synchronization losses equaled 320 or more.

The following PRM test results require the 310-9A Enhanced ESF/DS1 Timing Slips Option.

FAR FRM ES

Far-End Frame Error Seconds — The number of seconds during which one or more frame errors occurred in the far-end received signal. This result reports on the PRM Frame-Synchronization-Bit Error Event Bit (FE = 1) status.

FAR FRM SES

Far-End Severely Errored Framing Seconds —The number of seconds during which two or more frame errors occurred in less than 3 ms in the far-end received signal. This result reports on the PRM Severely-Errored Framing Event Bit (SE = 1) status.

FAR SLIP SEC

Far-End Controlled Slip Seconds —The number of seconds during which controlled slips occurred in the far-end received signal. This result reports on the PRM Controlled-Slip Event Bit (SL = 1) status.

PAYLOAD SOURCE

Far-End Payload Source/Loopback —Identifies the direction of the PRM according to the PRM Command/Response Bit (C/R) and the Payload Loopback Activated Bit (LB). In end-to-end applications, a customer-generated PRM is indicated as CUST (C/R = 0 and LB = 0), and the carrier-generated PRM is indicated as CARR (C/R = 1 and LB = 0) in the display. In payload loopback applications, the customer-generated PRM is indicated as CUST LOOP (C/R = 0 and LB = 1) when the customer is looped back, and the carrier-generated PRM is indicated as CARR LOOP (C/R = 1 and LB = 1) when the carrier is looped back.

FAR CRC ERR

Far-End CRC Error Events — The minimum number of CRC errors reported in the following FCRC results. A">" (greater than) preceding the count indicates that the Bins 2 through 6 are non-zero. This result reports on the PRM CRC Error Event Bits (G1 to G6) status.

FCRC 1

Far-End CRC 1 Bin — The number of seconds during which only one CRC error was reported in the far-end received signal. This result reports on the first PRM CRC Error Event Bit (G1 = 1) status.

FCRC 2-5

Far-End CRC 2 to 5 Bin — The number of seconds during which 2 to 5 CRC errors were reported in the far-end received signal. This result reports on the second PRM CRC Error Event Bit (G2 = 1) status.

FCRC 6-10

Far-End CRC 6 to 10 Bin —The number of seconds during which 6 to 10 CRC errors were reported in the far-end received signal. This result reports on the third PRM CRC Error Event Bit (G3 = 1) status.

FCRC 11-100

Far-End CRC 11 to 100 Bin — The number of seconds during which 11 to 100 CRC errors were reported in the far-end received signal. This result reports on the fourth PRM CRC Error Event Bit (G4 = 1) status.

FCRC 101-319

Far-End CRC 101 to 319 Bin — The number of seconds during which 101 to 319 CRC errors were reported in the far-end received signal. This result reports on the fifth PRM CRC Error Event Bit (G5 = 1) status.

FCRC >319

Far-End CRC 320 to 333 Bin —The number of seconds during which 320 to 333 CRC errors were reported in the far-end received signal. This result reports on the sixth PRM CRC Error Event Bit (G6 = 1) status.

13.7 SIGNAL CATEGORY

SIG L SEC

Signal Loss Seconds — The number of seconds during which the received DS1 signal was lost for all or part of a second since initial signal detection.

RX FREQ

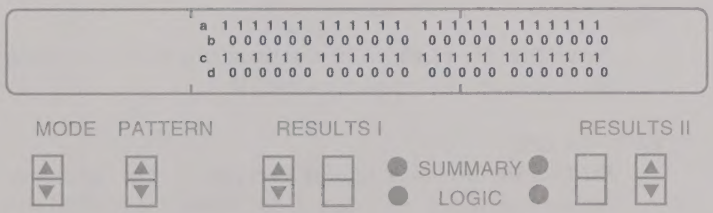
Receive Frequency — The frequency of the clock recovered from the received data measured in Hz.

RX LVL dBdsx

Receive Signal Level — The level of the received DS1 signal in dB relative to a standard 3-volt base-to-peak signal (DSX level).

abcd

ABCD Channel Signaling Status — The result displays the channel signaling bits for all 24 DS0 channels in D4 or SLC-96 (A and B) and ESF or ZBTSI (A, B, C, and D) framing. Scrolling to this result causes the entire display (both lines) to show the signaling bit states for each DS0 channel. The signaling bits are displayed as shown. "N/A" appears in channels C and D when D4 or SLC-96 framing is selected.



VF LVL dBm

Received Signal Level in dBm —The level of the average power in the currently selected DS0 channel (see **DS0 DROP CHANNEL** switch).

TIMING SLIPS

DS1 Timing Slips — The number of bit slips and frame slips counted when the DS1 test signal slips (+ or -) from the DS1 reference signal after both signals are present simultaneously.

13.8 TIME CATEGORY

TIME

Current Time of Day — The current time of day in hours, minutes, and seconds. The time is set through the SET TIME auxiliary function.

DATE

Current Date — The current day and month. The date is set through the SET DATE auxiliary function.

ELAPSED TIME

Elapsed Time — The elapsed time in hours, minutes, and seconds since the last 310-1 test restart.

TEST LENGTH

Timed Test Length — The currently set test length for a timed test in hours and minutes on the 310-1. The test length is set through the TEST LENGTH auxiliary function.

TIME LEFT

Timed Test Time Left —The time remaining for a timed test in hours, minutes, and seconds on the 310-1.

FAR PRM SEC

Far-End Performance Report Seconds — The number of total seconds, since test restart, during which a valid PRM was received. Requires the 310-9 Enhanced ESF Analysis Option.

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